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MS-AC951

Ver: 1.0

Intel Sharkbay plamform H81

CPU: INTEL-Haswell LGA1150

System Chipset: INTEL-LYNX

Memory: DDRIII SO-DIMM (1333/1666MHz) * 2
(Dual Channel)

GPU: NVIDIA N14P-GV2
NVIDIA N14M-GE/GL

CPU PWM: VRD12 - ISL95812

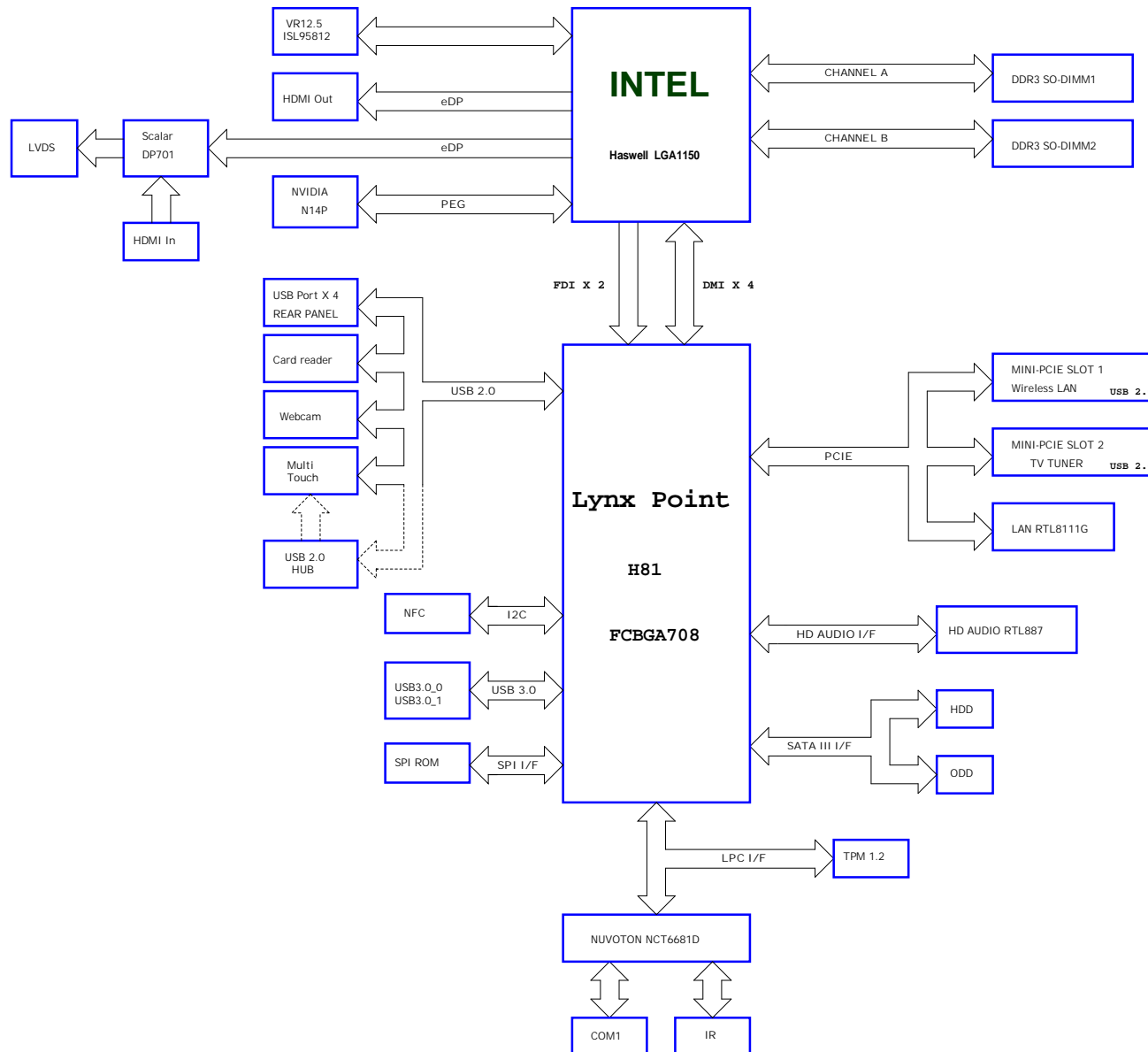
OnBoard Chipset: SIO NUVOTON NCT6681D
HD Audio Codec RTL887
LAN-realtek 8111G
CARD READER_RTS5139
SPI ROM: 64 MB
USB 2.0 Hub

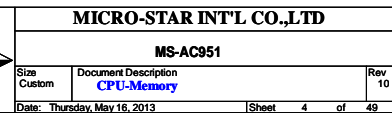
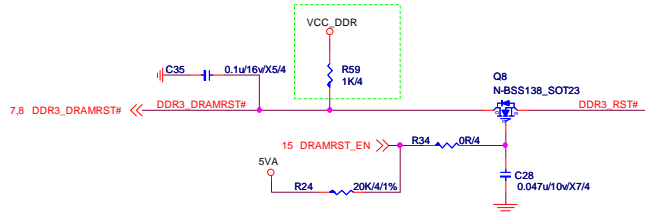
Expansion Slots: Mini PCI Express Slot * 2

Other: HDMI In *1
HDMI Out *1
SATA3 *2 , SATA2 *2
Side USB3.0 *2
REAL USB2.0 *4
COM Port *1

MS-AC951 Block Diagram

Intel Sharkbay platform H81





GND

GND



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MS-AC951

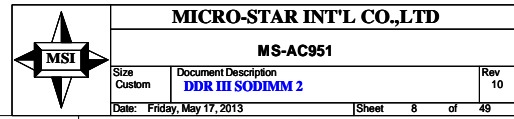
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SO DIMM1 #A

H=5.2mm

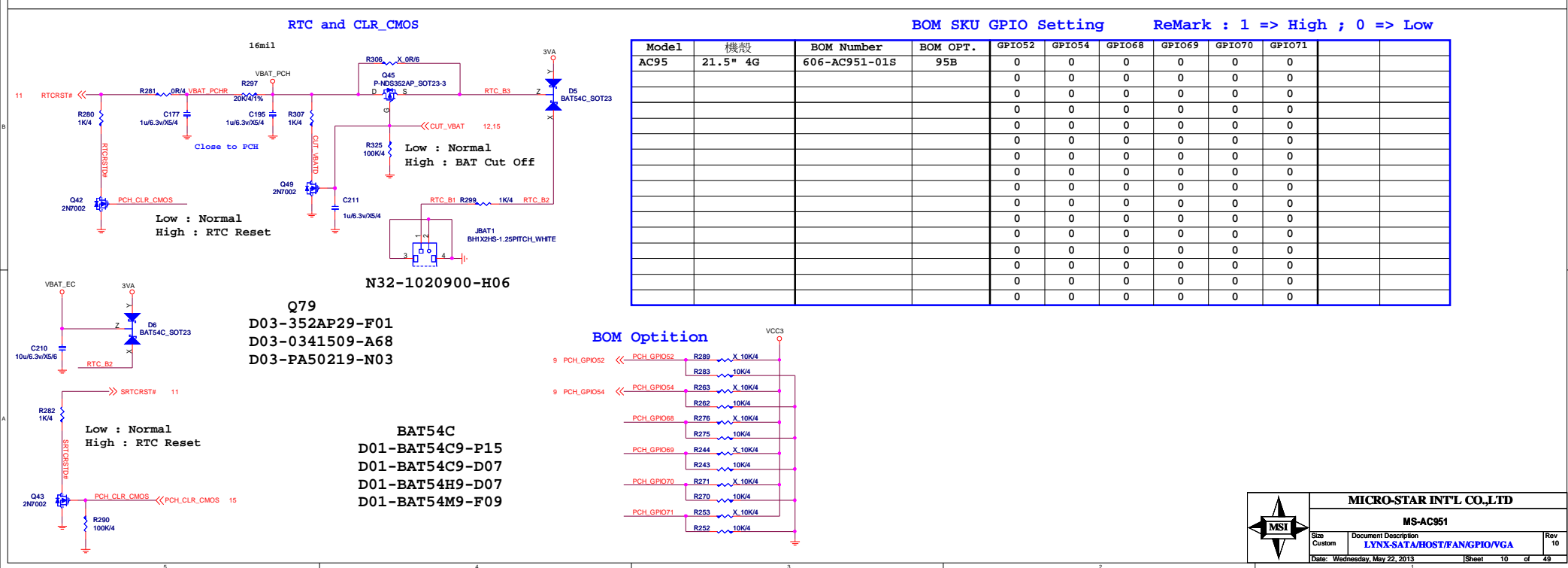


H=11mm

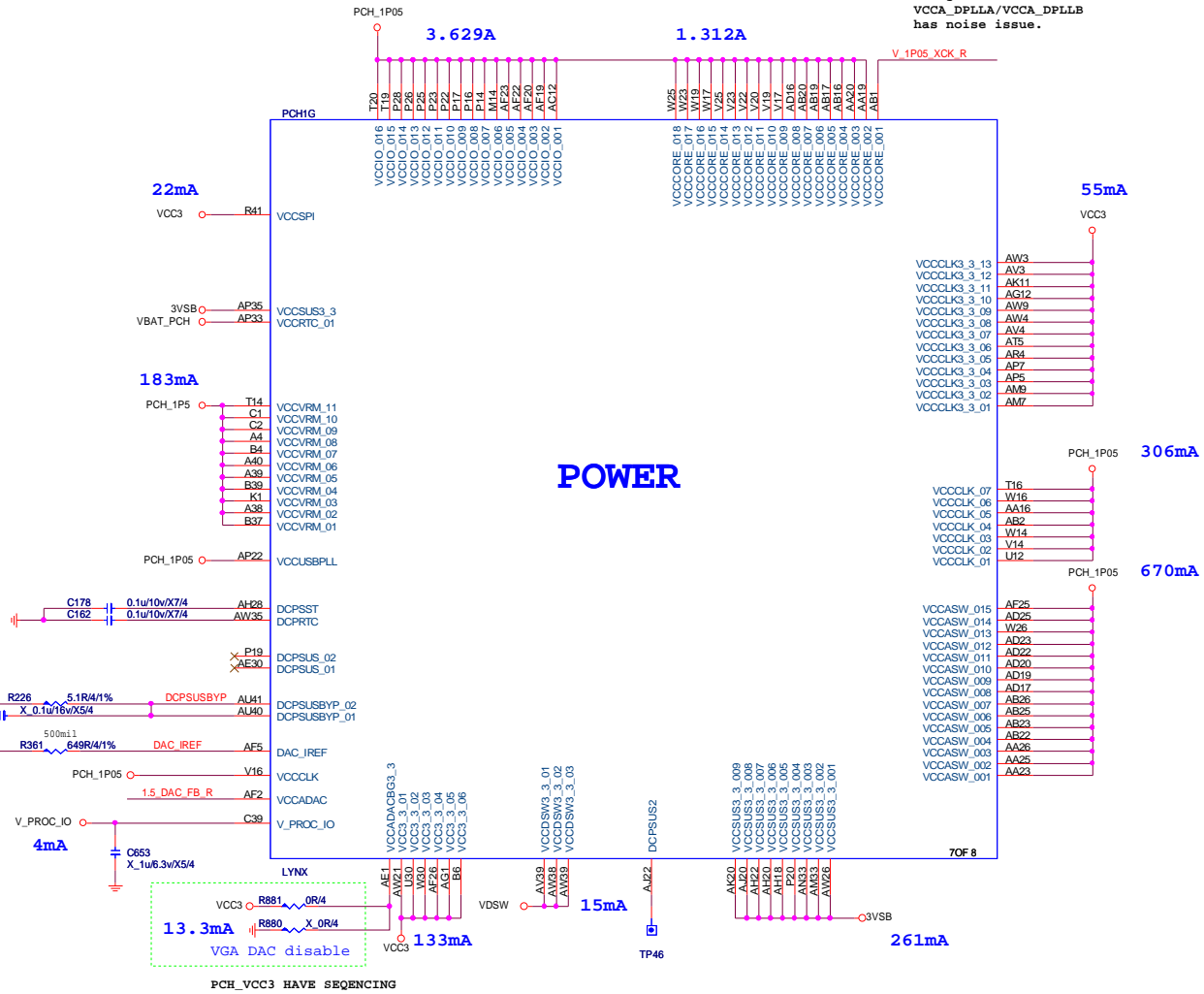
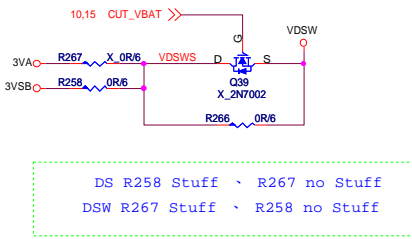
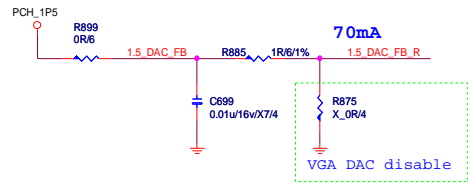
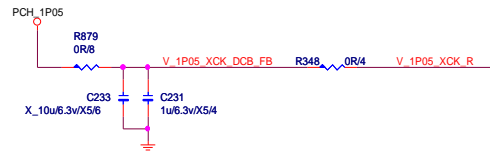



```
pcie port7,8 NA
```

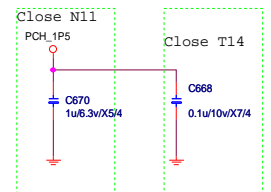
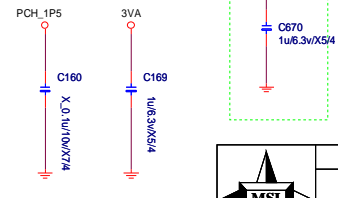
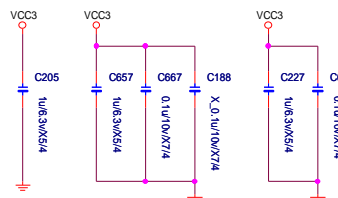
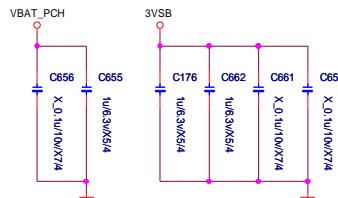
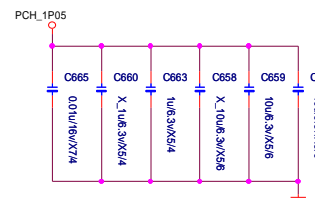
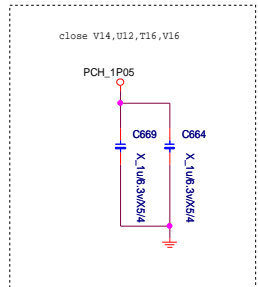


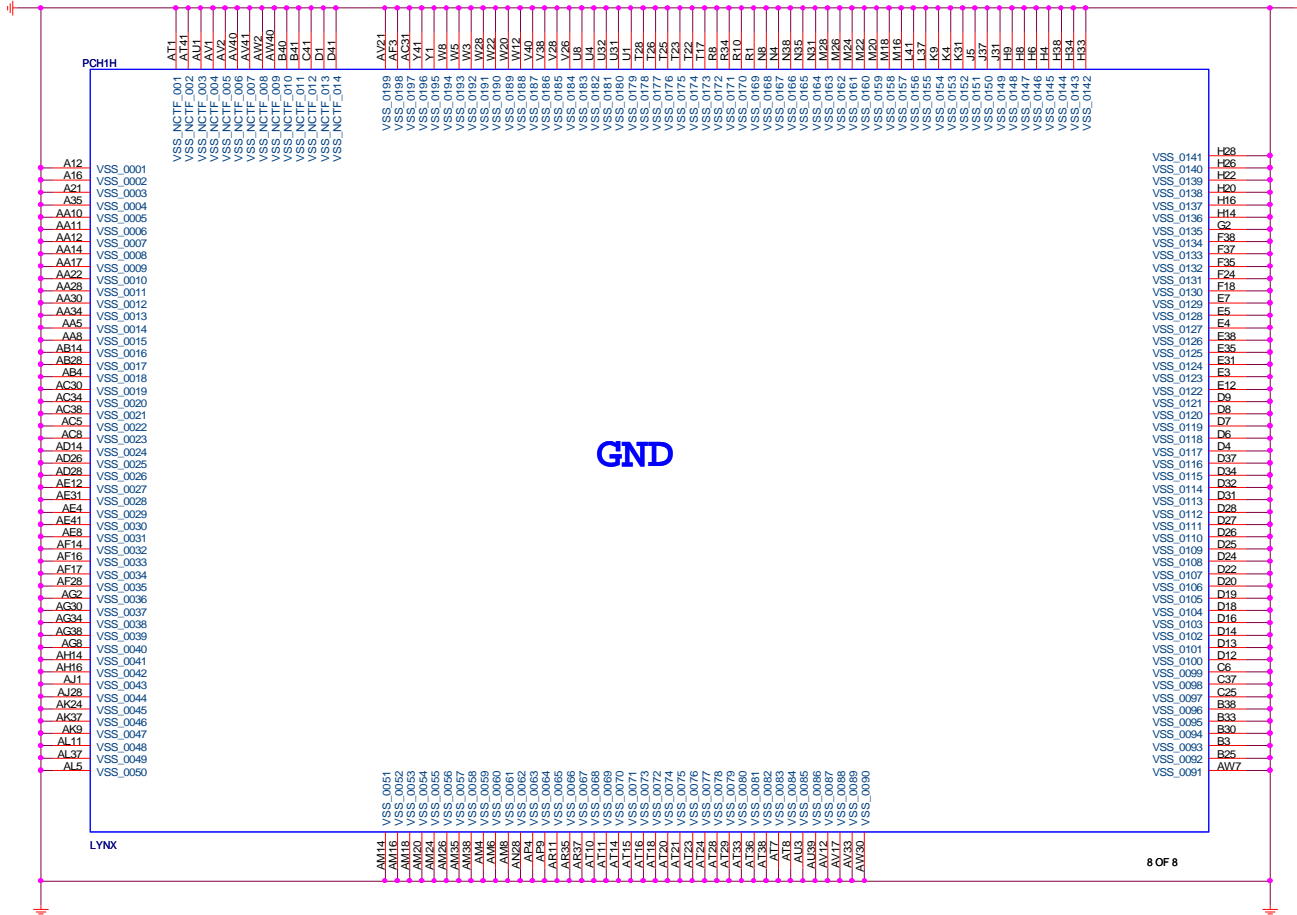


VCC3 0.223A
3VA 0.015A
VBAT 6uA
3VSB 0.261A
VCC1_5 0.253A
PCH_1P05 5.921A



PCH decoupling cap





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MS-AC951

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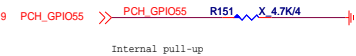
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PCH Straps



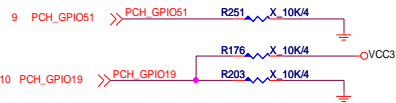
SPKR

Default Mode:
Internal weak Pull-down.
No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



GPIO55

Default Mode:
Internal pull-up.
Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GP/GPIO19, GPIO51

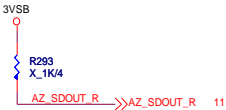
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.
Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.
Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

Boot device	GPIO51	GPIO19
LPC	0	0
SPI	1	1



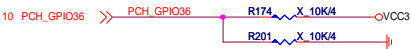
GPIO53

Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.



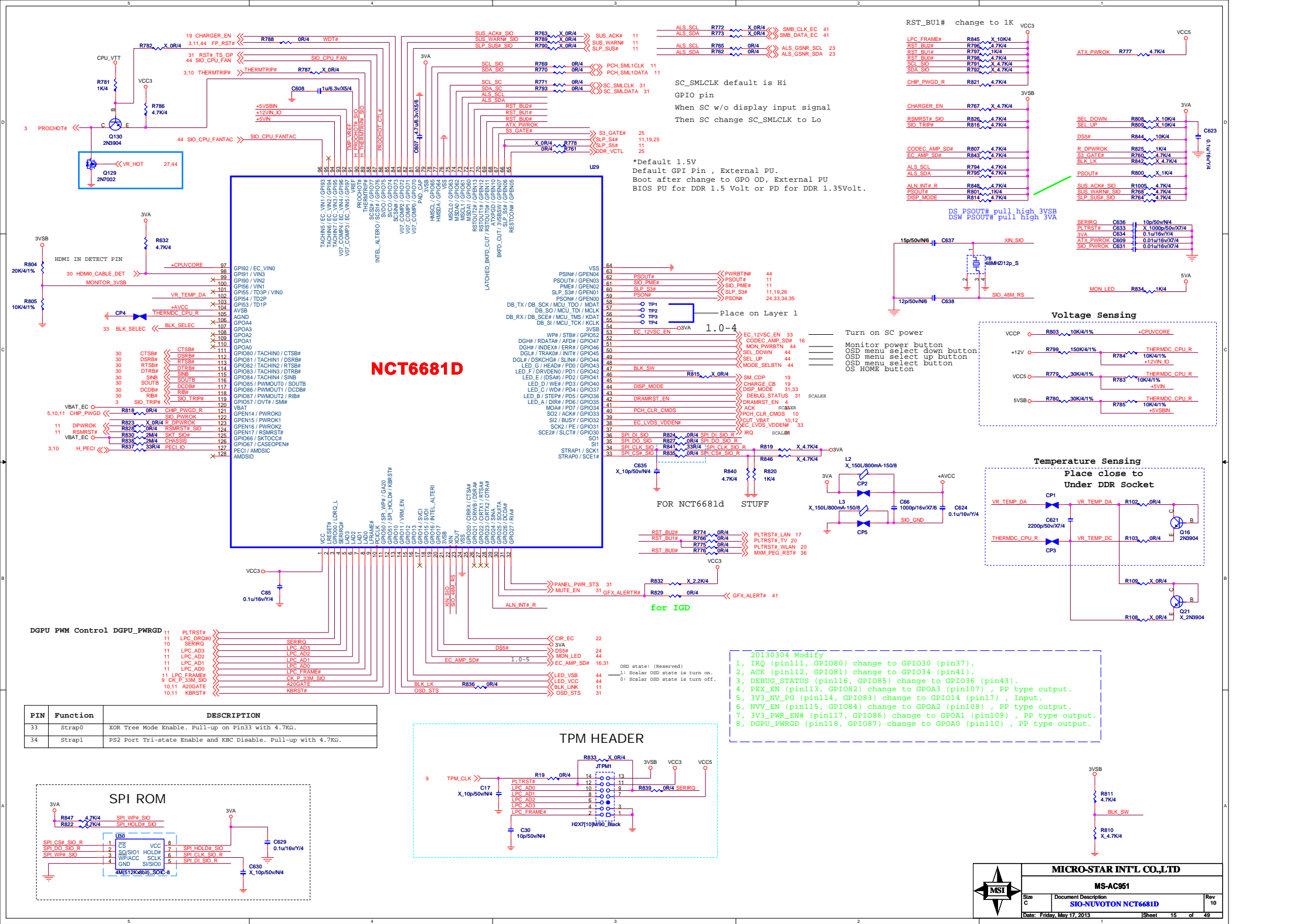
HDA_SDO

Default:
Do not pull high.
Disable MB in Manufacturing Mode:
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

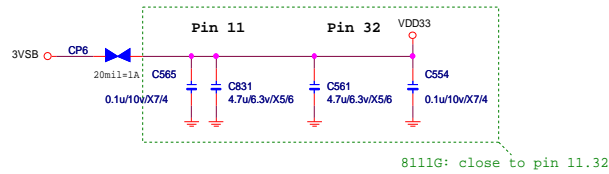
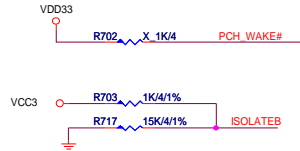


GPIO37

Enable TLS:
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

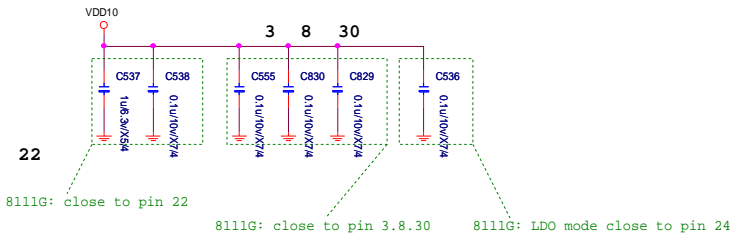


RTL8111G Giga LAN



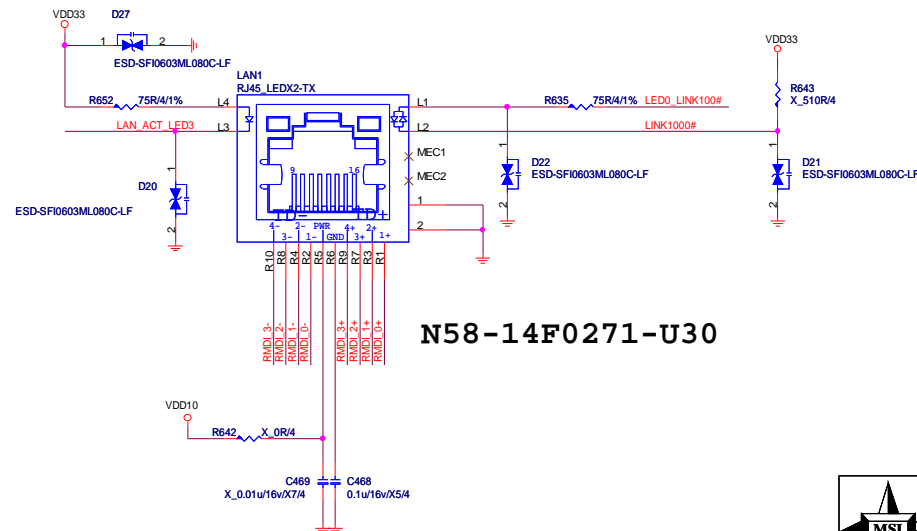
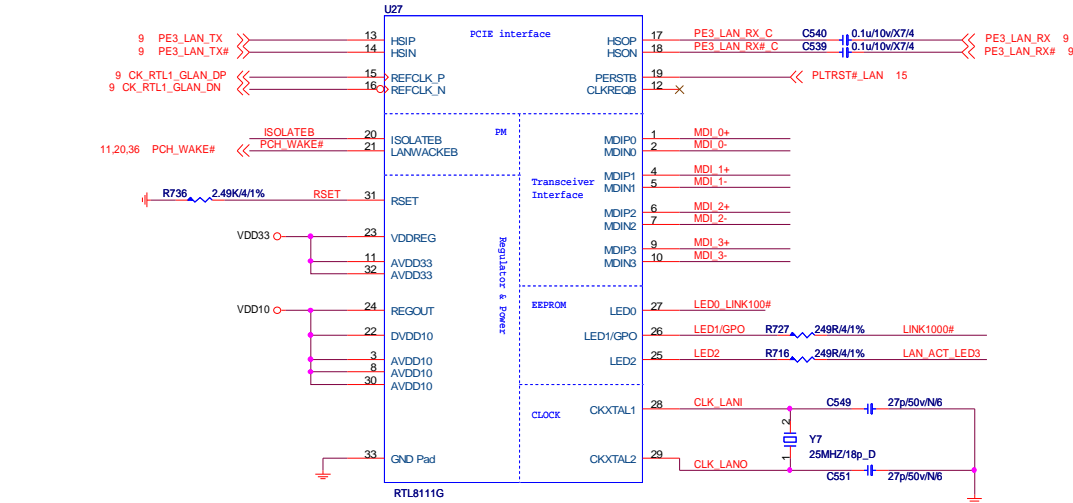
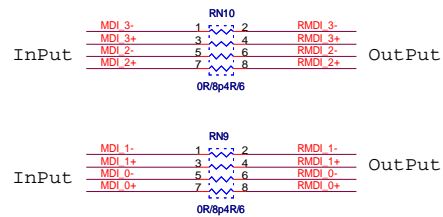
8111G: close to pin 11.32

Icc33 average operating supply current from 3.3V
At 1Gbps with heavy network traffic 70mA

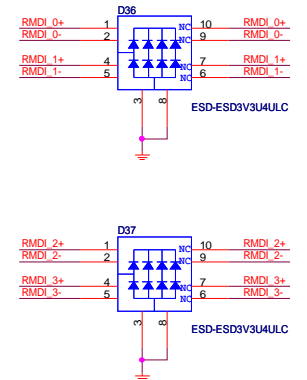


8111G: close to pin 22
8111G: close to pin 3.8.30
8111G: LDO mode close to pin 24

Icc10 average operating supply current from 1.0V
At 1Gbps with heavy network traffic 300mA



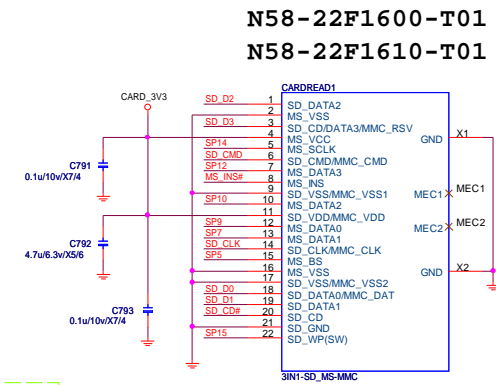
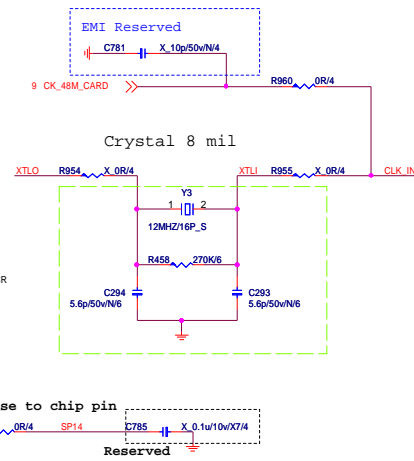
Reserve ESD Protect
for connector



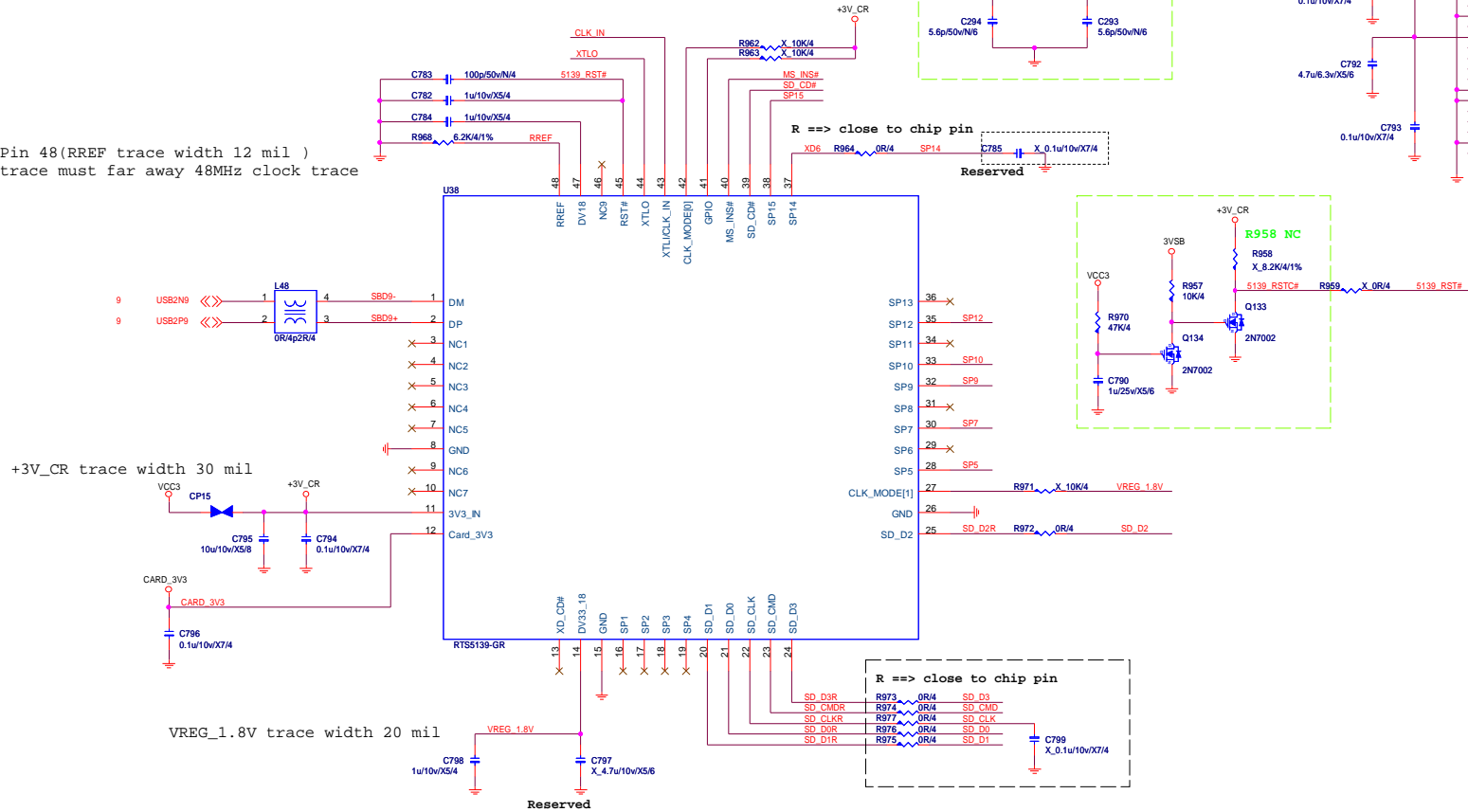
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Custom	LAN RTL8111G	10	
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Pin 48(RREF trace width 12 mil)
trace must far away 48MHz clock trace

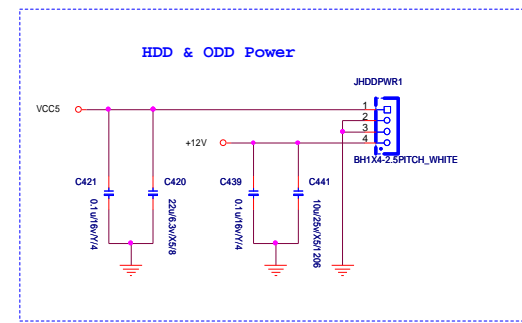
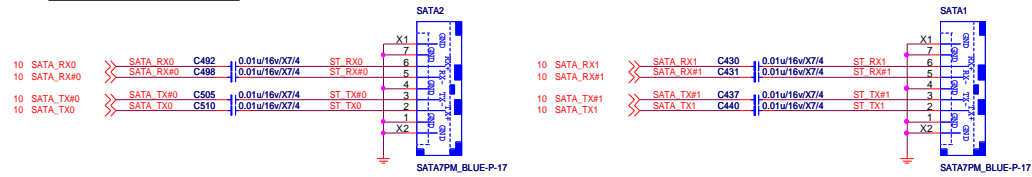
CLK	MODE1 Pin 27 R971	MODE0 Pin 42 R962
48MHz	X	X
24MHz	X	1
12MHz (XTAL)	1	1



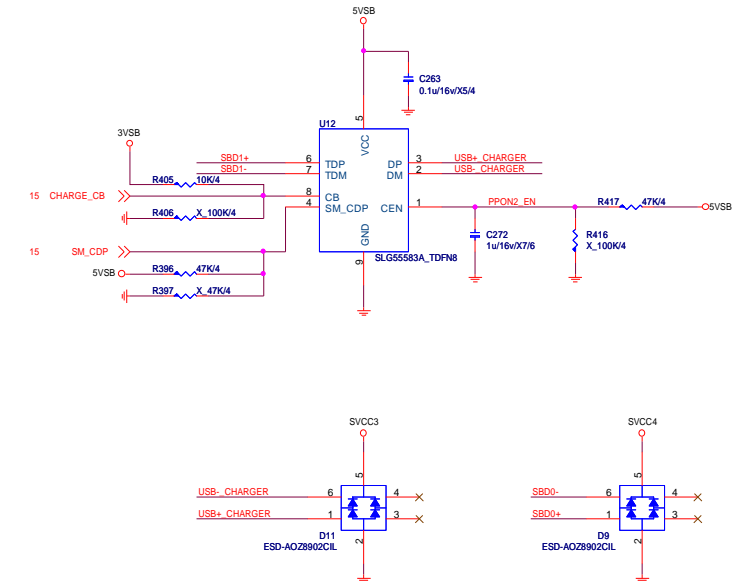
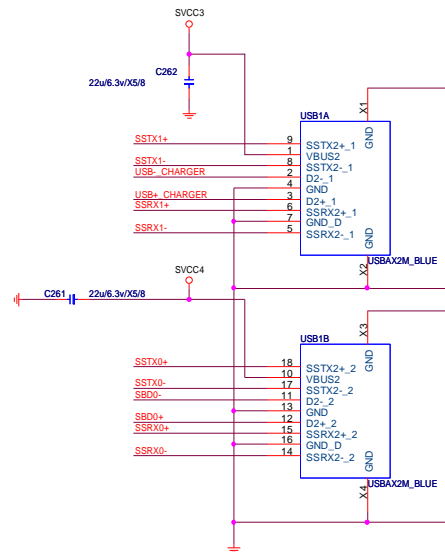
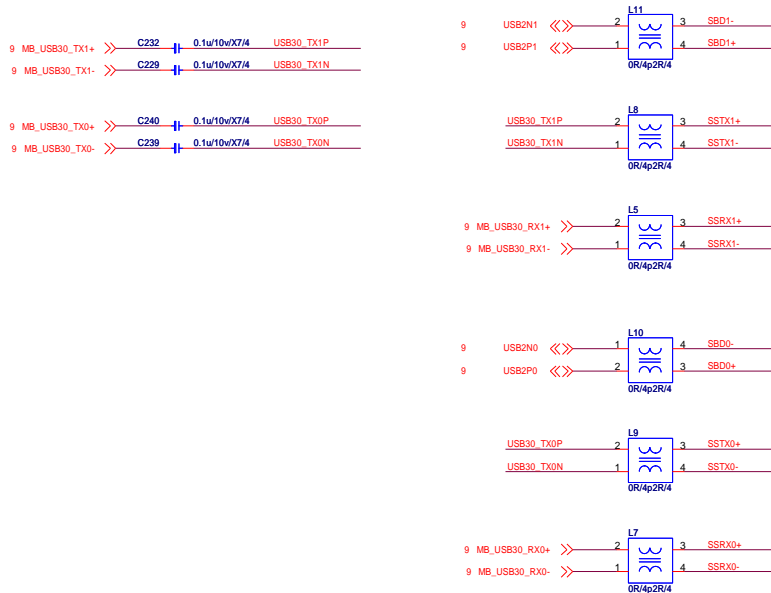
SP1=SD_D7	/	xD_RDY	n/a
SP2=SD_D6	/	xD_RE#	n/a
SP3=SD_D5	/	xD_CSE#	n/a
SP4=SD_D4	/	xD_W#	n/a
SP5=MS_B8 / xD_CLE			
SP6=MS_D5	/	xD_ALE	n/a
SP7=MS_D1 / xD_WP#			
SP8=MS_D4	/	xD_D0	n/a
SP9=MS_D0	/	xD_D1	
SP10=MS_D2	/	xD_D2	
SP11=MS_D6	/	xD_D3	n/a
SP12=MS_D3	/	xD_D4	
SP13=MS_D7	/	xD_D5	n/a
SP14=MS_CLK	/	xD_D6	
SP15=SD_WP	/	xD_D7	



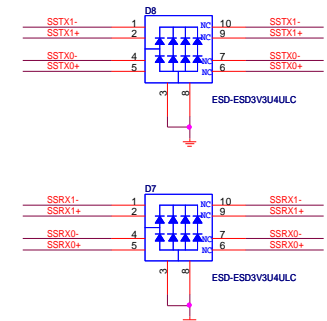
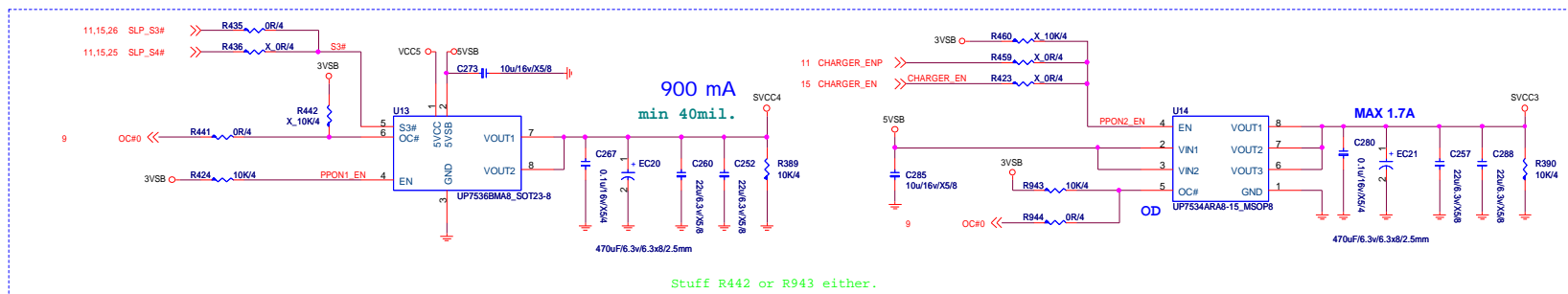
SATA 6G PORT 0,1



USB 3.0 PORT 0,1



USB3.0 & USB2.0 SKU POWER KEEP

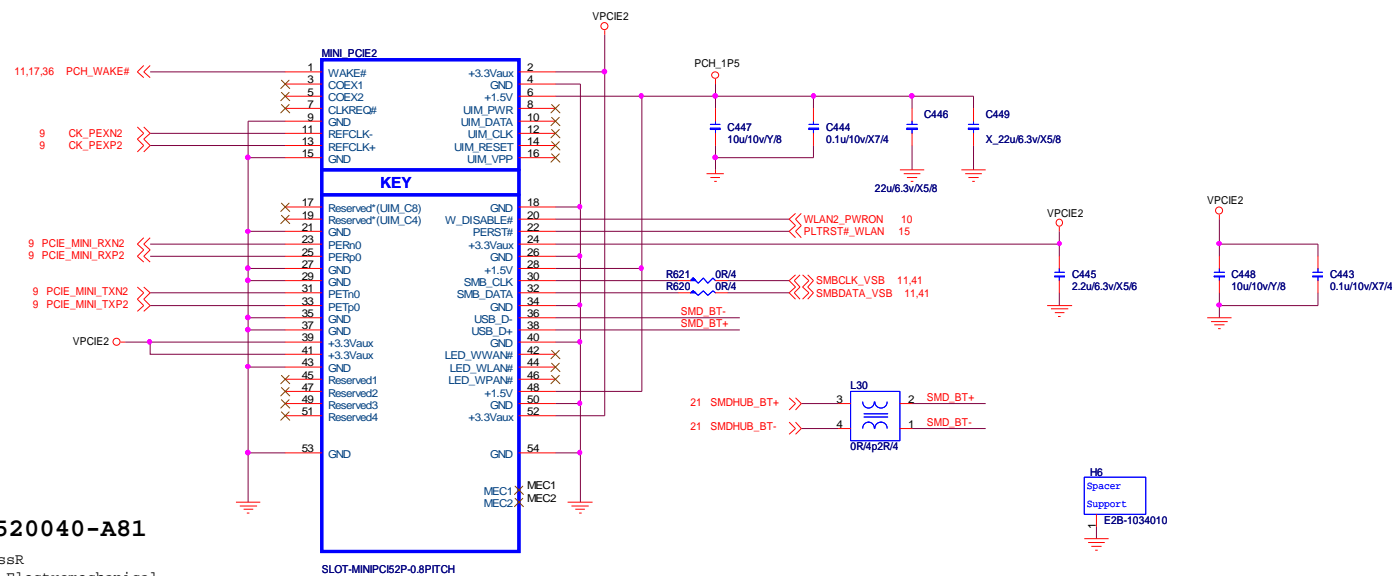


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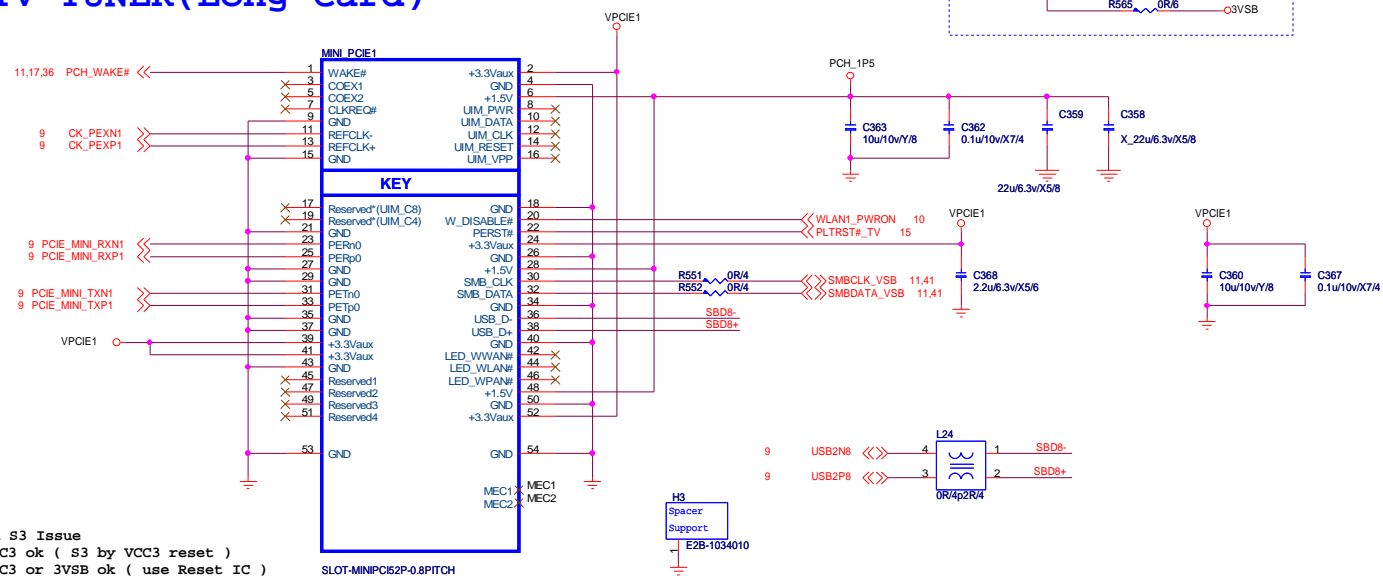
MS-AC951

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Wireless LAN(Short Card)

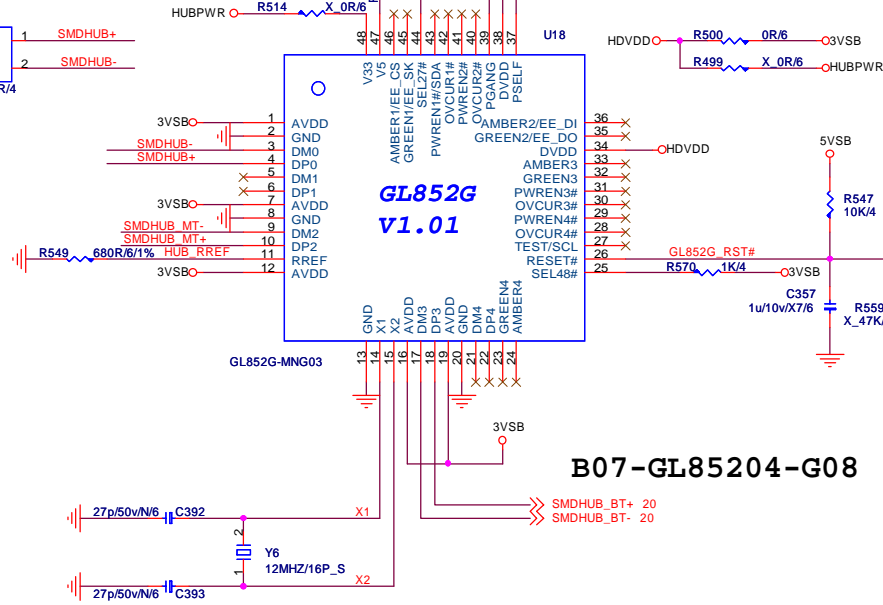
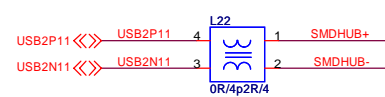
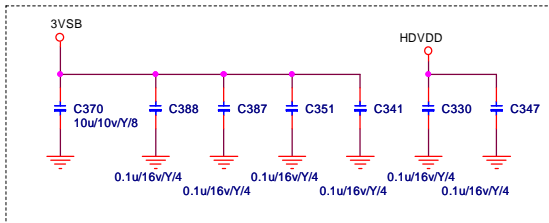


TV TUNER(Long Card)

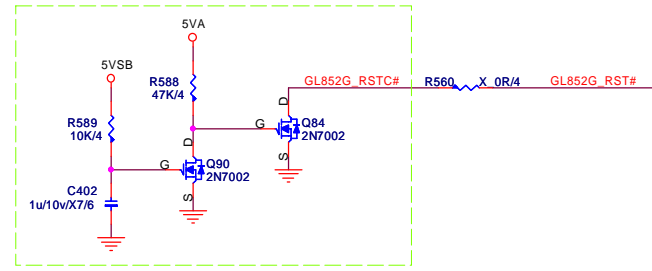
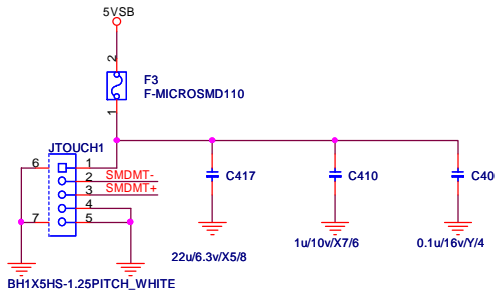
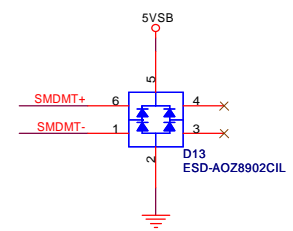
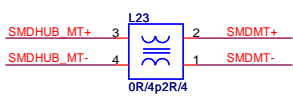
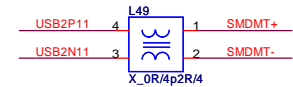


圖例 TV-Card S3 Issue
H335A ==> VCC3 ok (S3 by VCC3 reset)
H335B ==> VCC3 or 3VSB ok (use Reset IC)

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Multi Touch

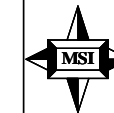


Clock and Reset Interface				
Pin Name	GL852G		I/O Type	Description
	48 Pin#	28 Pin#		
X1	14	10	I	Crystal / OSC clock input
X2	15	11	O	Crystal clock output.
RESET#	26	17	I	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.
SEL48#/SEL27#	25,44	--	I	SEL48#/SEL27#: 0 1: 48MHz OSC-in 1 0: 27MHz OSC-in 1 1: 12MHz X'tal/OSC-in

RREF	11	B	A 680Ω resistor must be connected between RREF and analog ground (AGND).
------	----	---	--

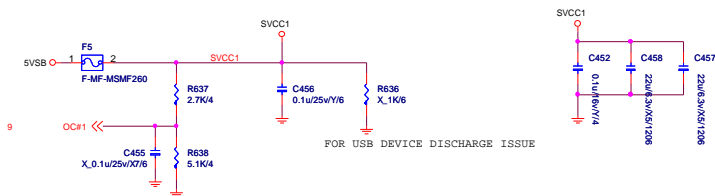
Power / Ground			
Pin Name	GL852G		Description
	48 Pin#	I/O Type	
AVDD	1,7,12,16,19	P	3.3V analog power input for analog circuits.
DVDD	34,38	P	3.3V digital power input for digital circuits
GND	2,8,13,20	P	Ground
V5	47	P / I	5V Power input. It need be NC if using external regulator
V33	48	P / O	5V-to-3.3V regulator Vout (LQFP48) It can be NC or connect to 3.3V power if using external regulator (LQFP48 only)

PSELF	37	I	0: GL852G is bus-powered. 1: GL852G is self-powered.
PGANG	39	B	This pin is default put in input mode after power-on reset. Individual/gang mode is strapped during this period. After the strapping period, this pin will be set to output mode, and then output high for normal mode. When GL852G is suspended, this pin will output low. *For detailed explanation, please see Chapter 5 Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend

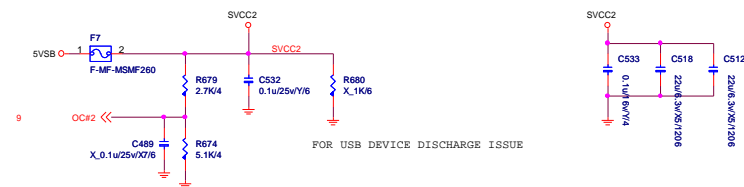


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Multi Touch / USB 2.0 Hub			
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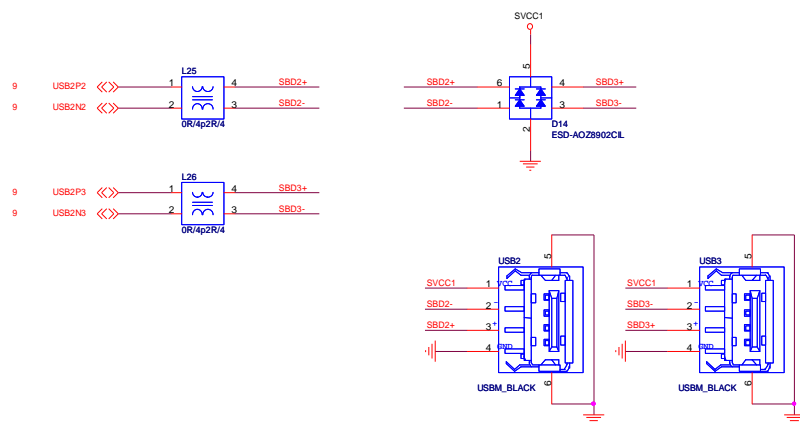
POWER CIRCUIT FOR USB PORT 0,1 (REAR)



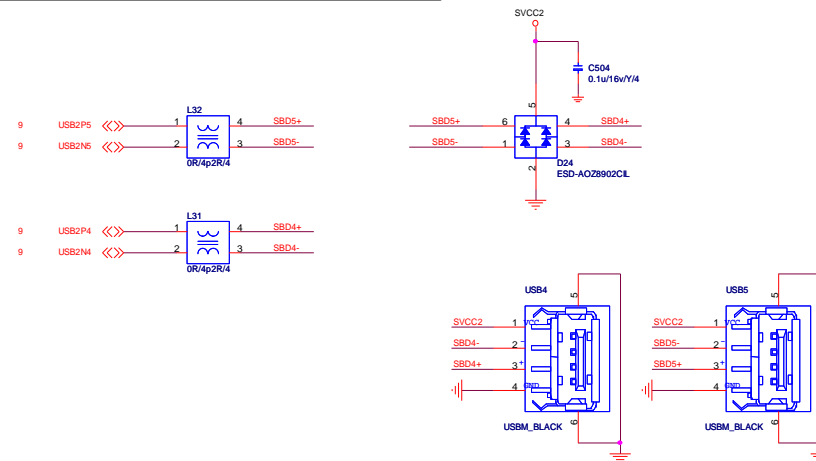
POWER CIRCUIT FOR USB PORT 2,3 (REAR)



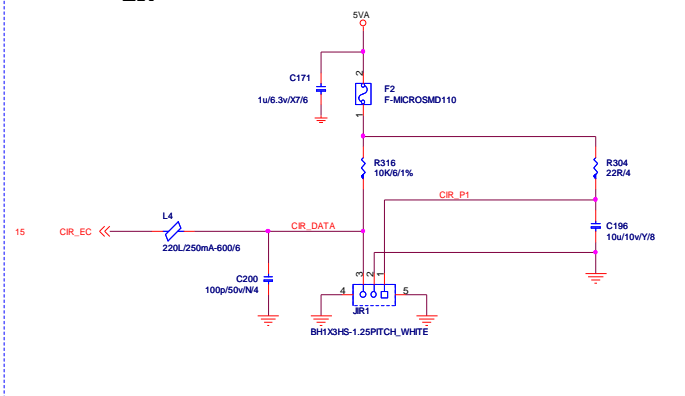
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



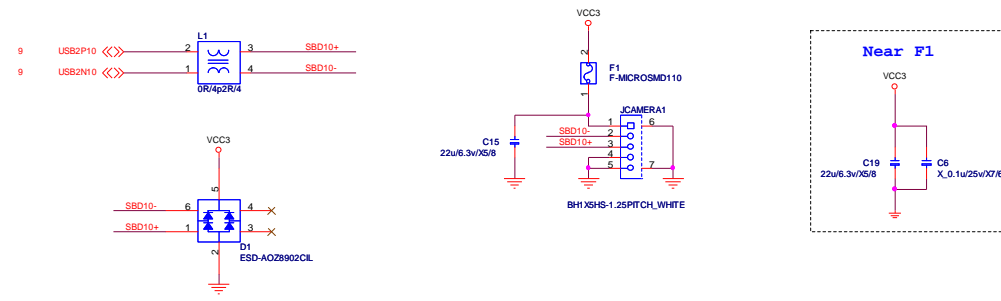
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



IR



Webcam

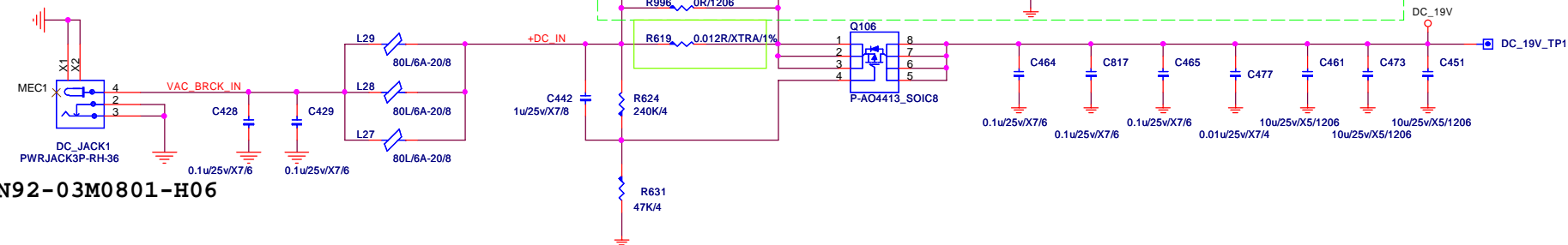


MICRO-STAR INT'L CO.,LTD

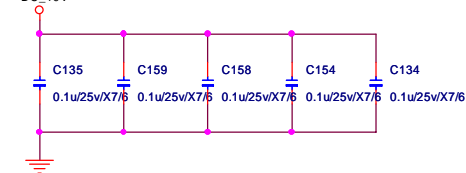
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N92-03M0801-H06



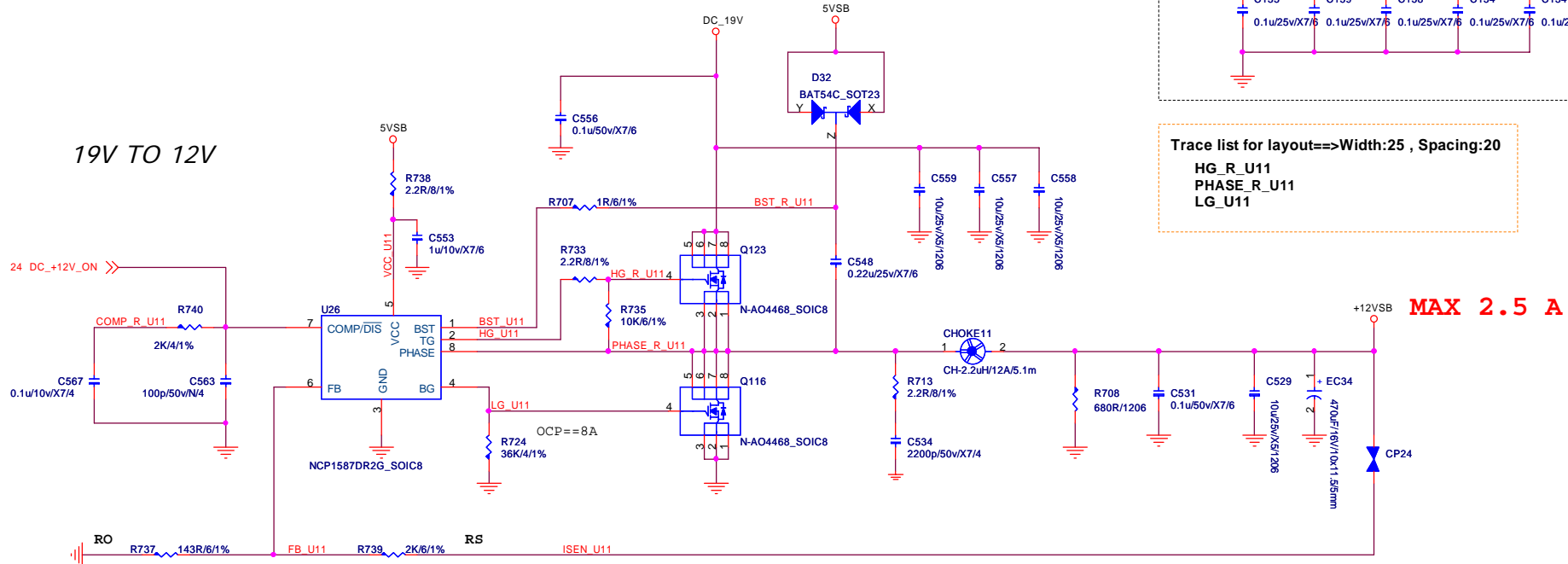
Reserve For EMI



Trace list for layout==>Width:25 , Spacing:20

HG_R_U11
PHASE_R_U11
LG_U11

19V TO 12V



$$V_{out} = 0.8 (1 + 2K / 143) = 11.989 \text{ Volt}$$

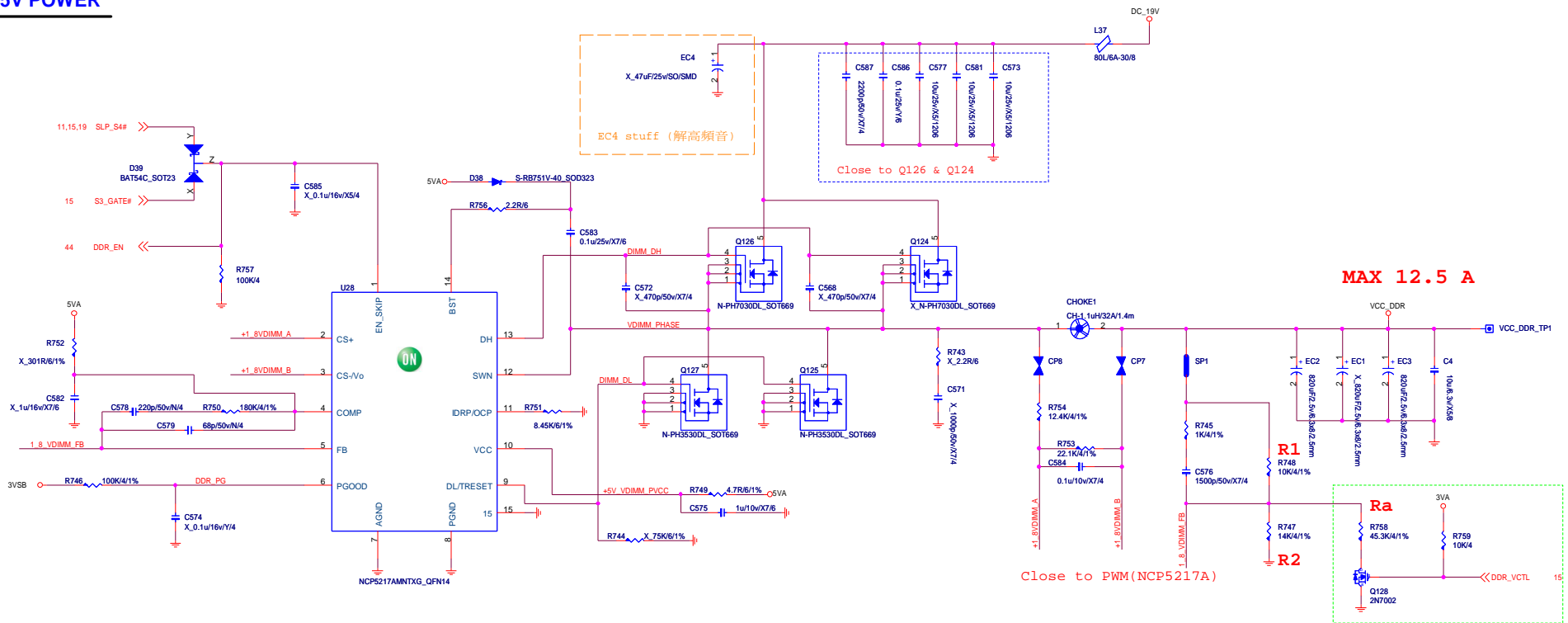


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DDR III 1.5V POWER

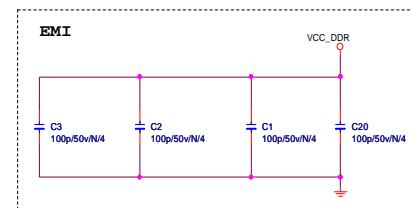
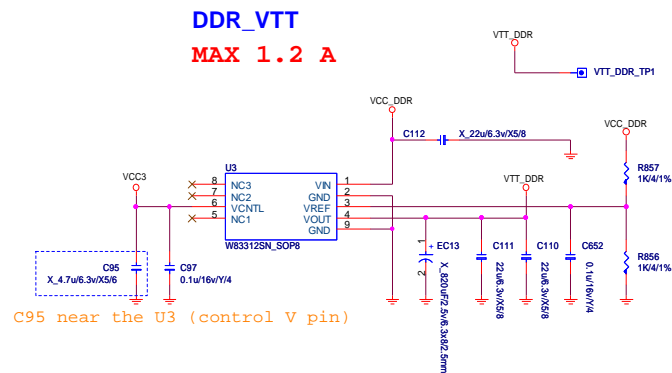


$$\begin{aligned} V_{CC_DDR} &= 0.8 \cdot \{1 + (R1 / (R2 // Ra))\} = 1.548 \text{ Volt} \\ V_{CC_DDR} &= 0.8 \cdot \{1 + (R1 / R2)\} = 1.371 \text{ Volt} \end{aligned}$$

*Default High / 1.5V

VCC_DDR	1.5 V	1.35 V
DDR_VCTL	High	Low

```
*Default 1.5V
Default GPI Pin , External PU.
Boot after change to GPO OD, External PU
BIOS PU for DDR 1.5 Volt or PD for DDR 1.35Volt.
```



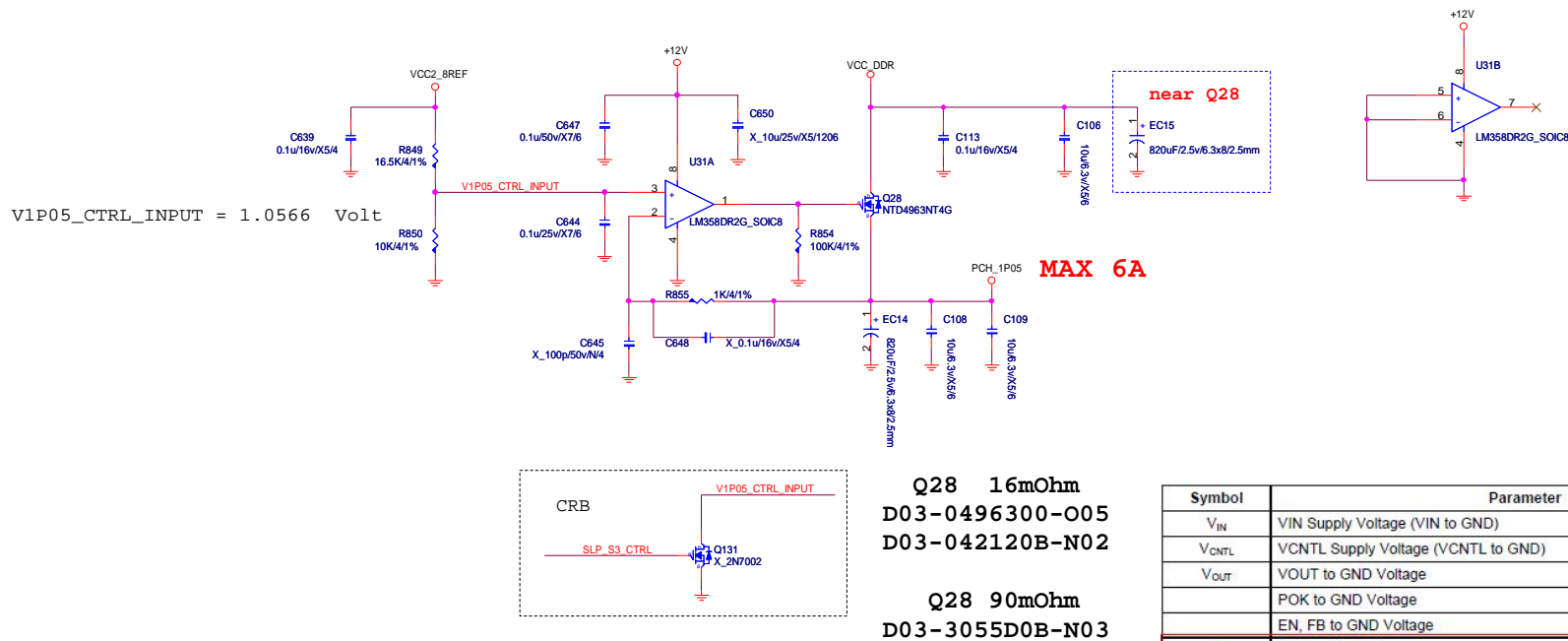
MICRO-STAR INT'L CO.,LTD

MS-AC951

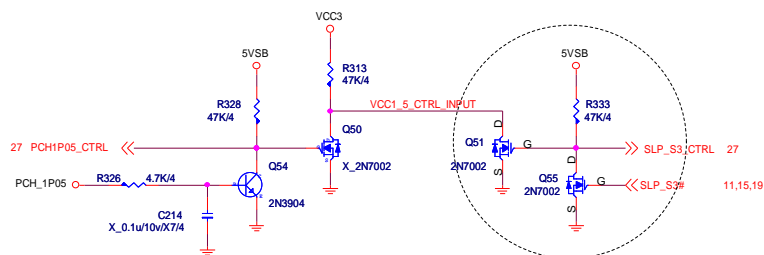
Size Custom	Document Description DDR POWER (NCP5217)
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Date: Thursday, May 16, 2013	Sheet 25 of 49
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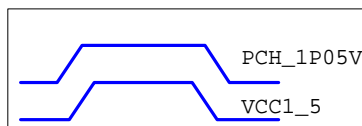
PCH Power:1.05V 5.917 A



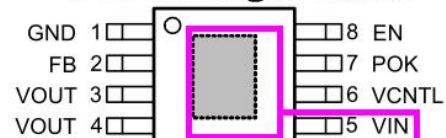
PCH Power:1.5V 0.253 A
Mini PCIE Power:1.5V 1 A



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

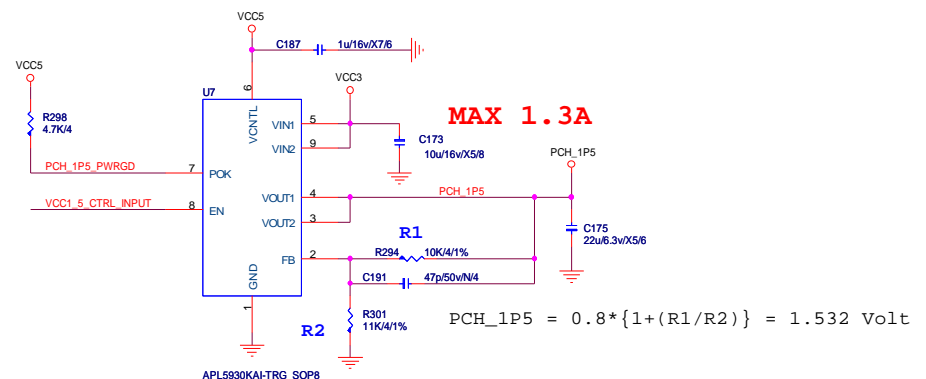


Pin Configuration



SOP-8P (Top View)

= Exposed Pad
(connected to VIN plane for better heat dissipation)



VCC3

R33
0R/4

VRD_EN

Q6
2N7002

Q4
X_2N7002

C18
X_0.1u/16v/X54

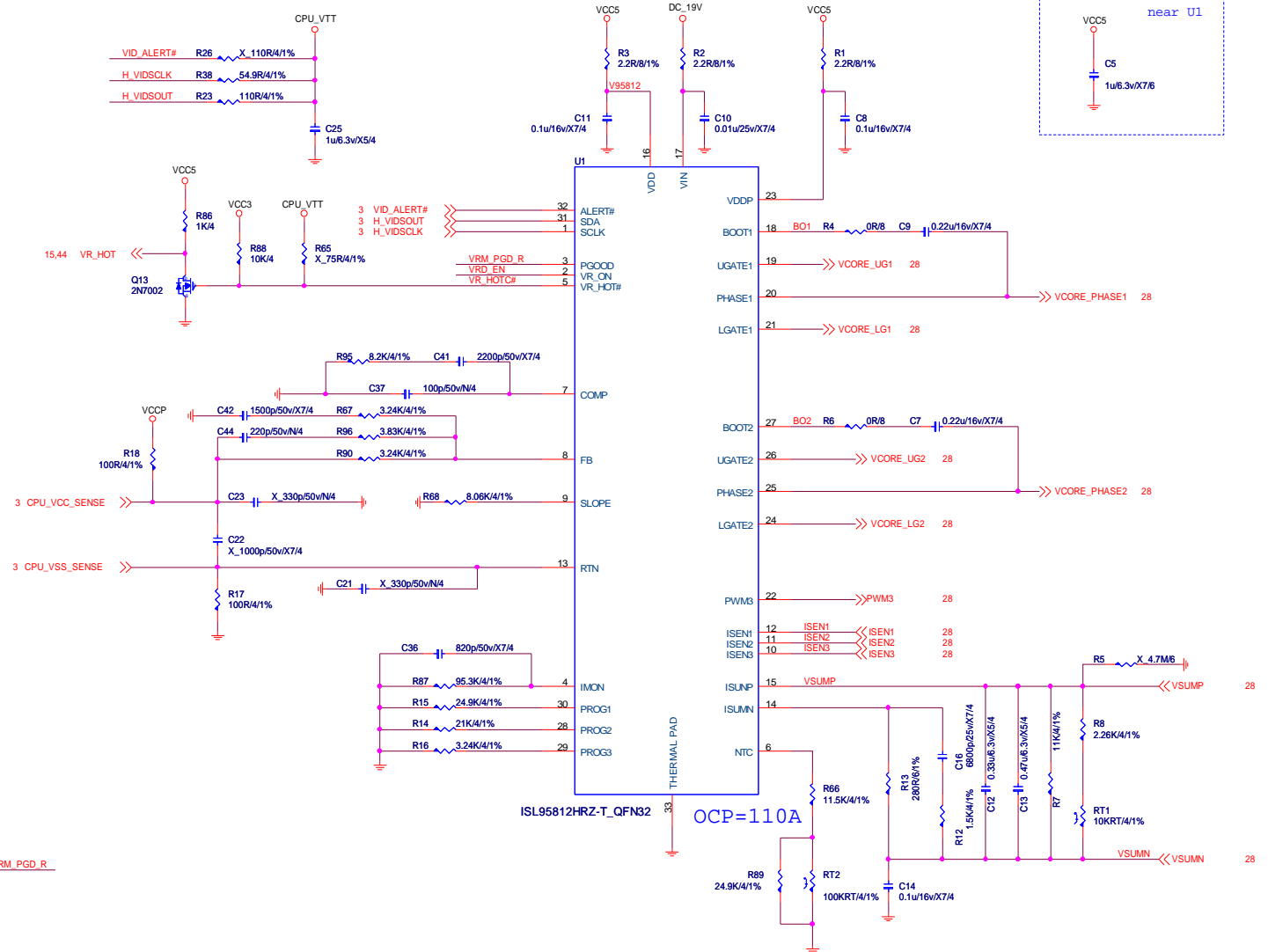
26 SLP_S3_CTRL

26 PCH1P05_CTRL

HIGH: 0.7V
LOW: 0.3V

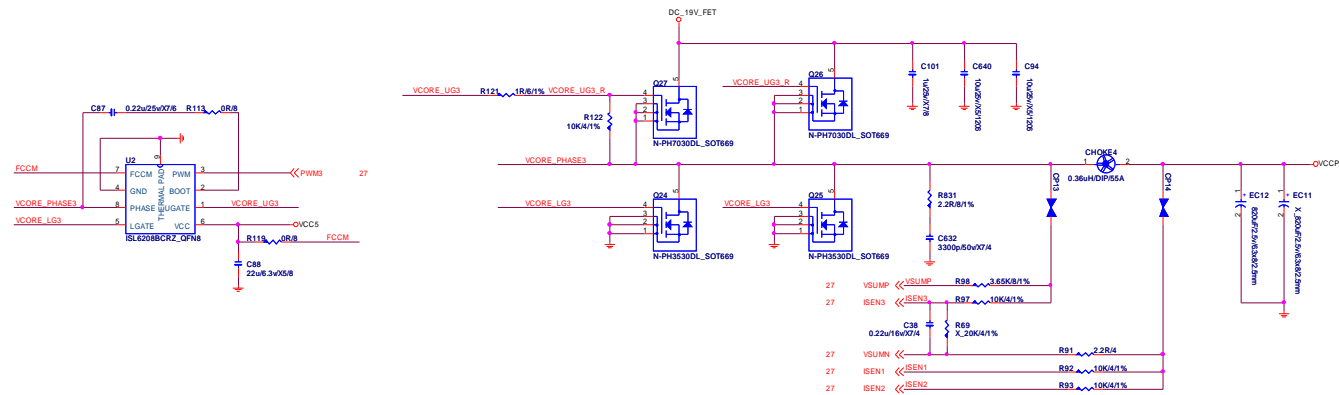
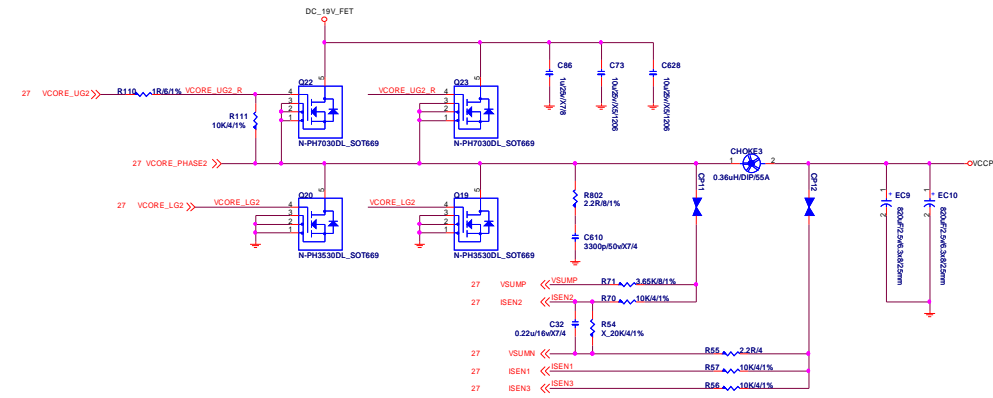
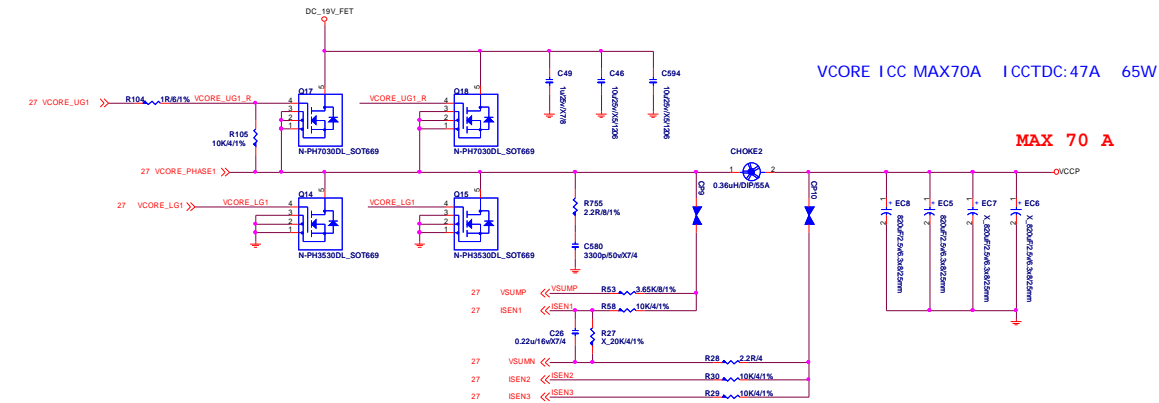
CRB

HIGH:by PCH_1P05V
LOW:by S3



Size Custom	Document Description CPU Power - ISL95812	Rev 10
Date: Thursday, May 16, 2013	Sheet 27 of 49	

VCCP POWER

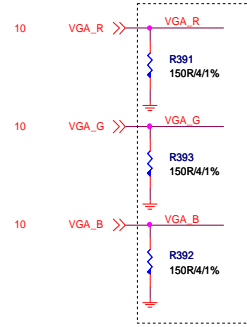


MICRO-STAR INT'L CO.,LTD

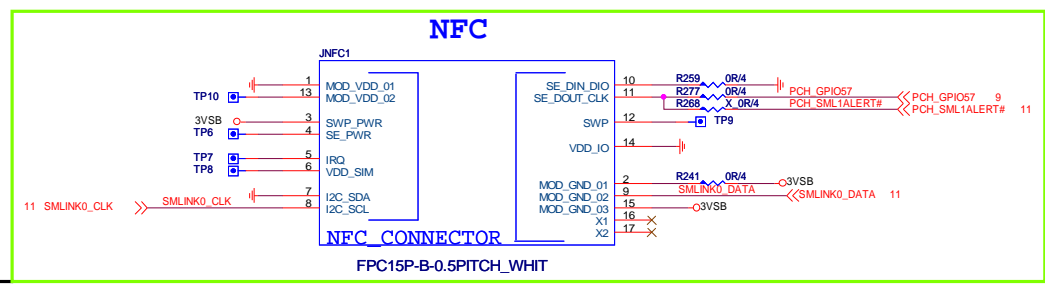
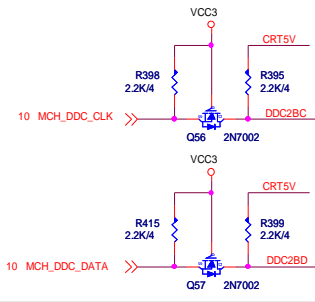
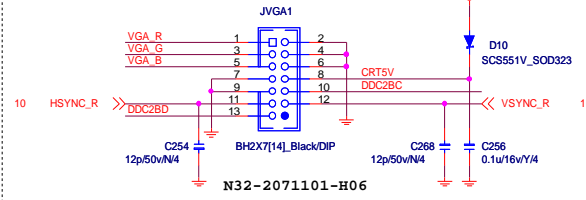
MS-AC951

Size	Document Description	Rev
Custom	CPU Power - MOSFET	10
Date: Thursday, May 16, 2013	Sheet 28 of 49	

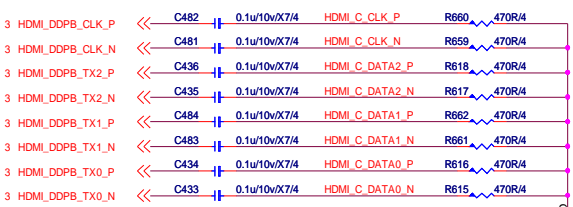
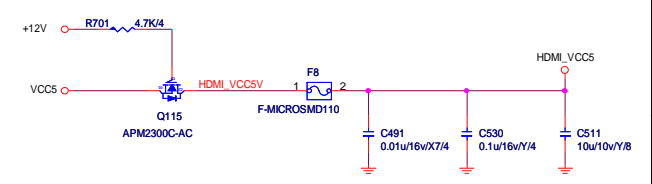
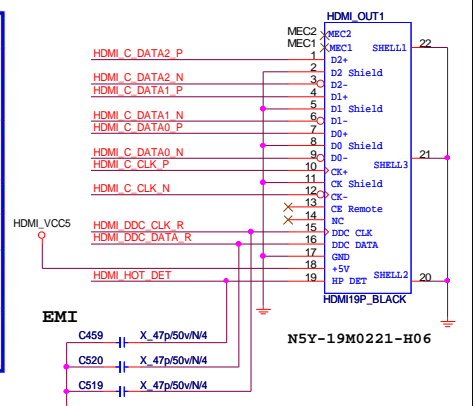
PLACE CLOSE TO VGA CONNECTOR
as close as possible to VGA connector within 500mil



VGA Connector (MP remove)

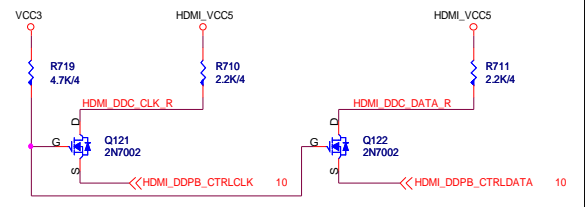
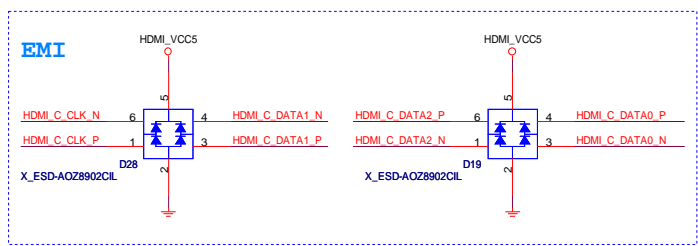
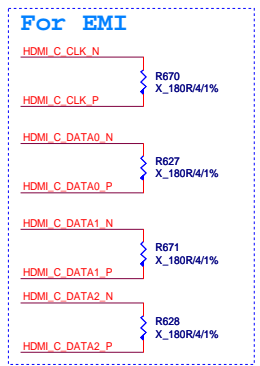


Valid Three Display Configurations through the Processor					
Display 1	Display 2	Display 3	Maximum Resolution Display 1	Maximum Resolution Display 2	Maximum Resolution Display 3
HDMI	HDMI	DP	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz		3840x2160 @ 60 Hz
DVI	DVI	DP	1920x1200 @ 60 Hz		3840x2160 @ 60 Hz
DP	DP	DP	3840x2160 @ 60 Hz		
VGA	DP	HDMI	1920x1200 @ 60 Hz	3840x2160 @ 60 Hz	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz
eDP	DP	HDMI	3840x2160 @ 60 Hz	3840x2160 @ 60 Hz	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz



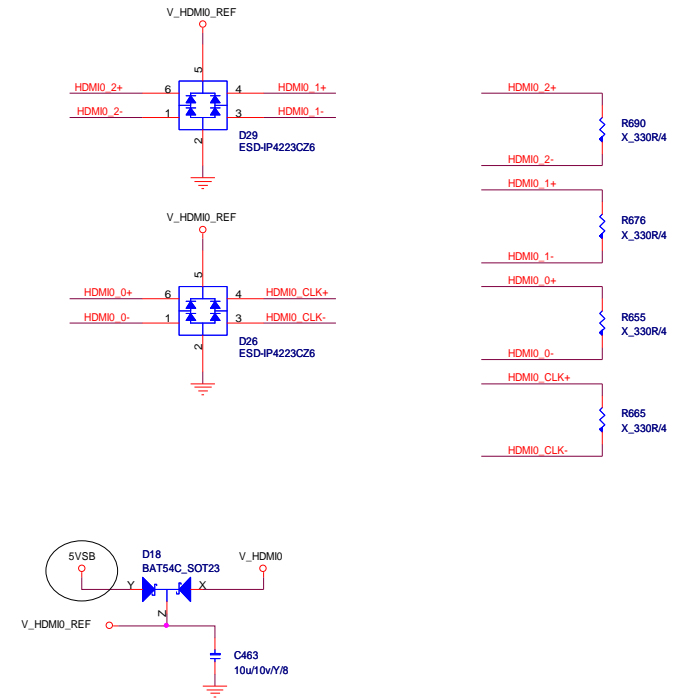
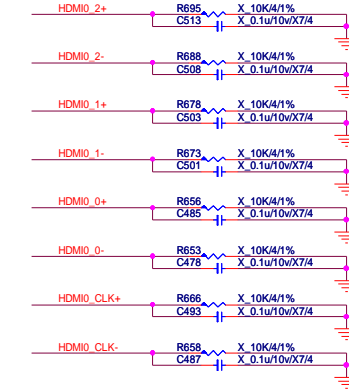
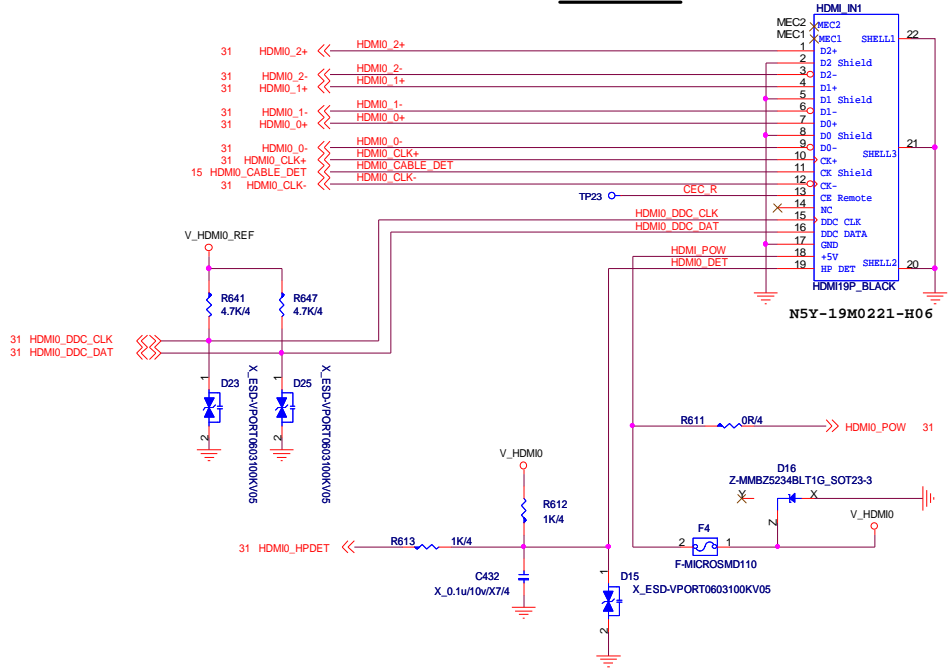
HDMI OUT

HDMI :
1920x1200 at 60 Hz (16:10 WUXGA)

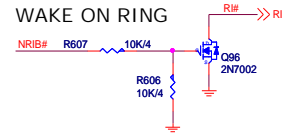
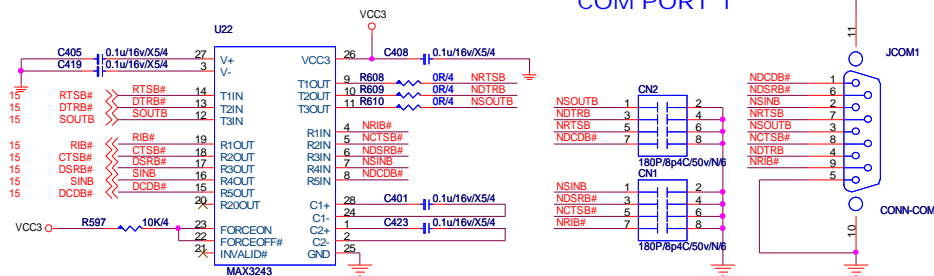


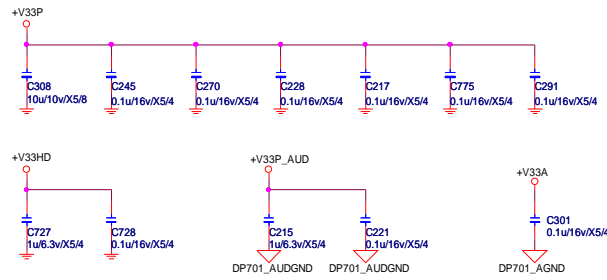
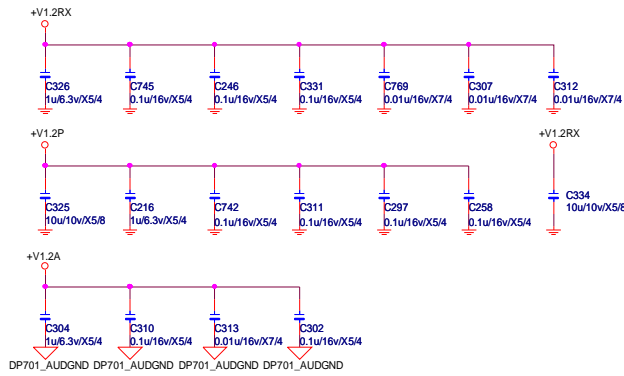
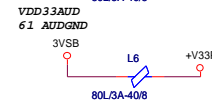
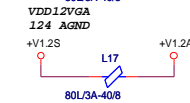
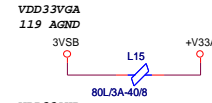
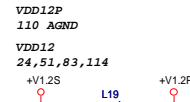
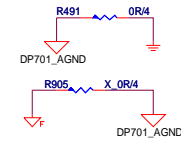
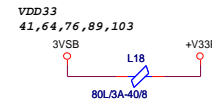
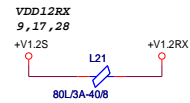
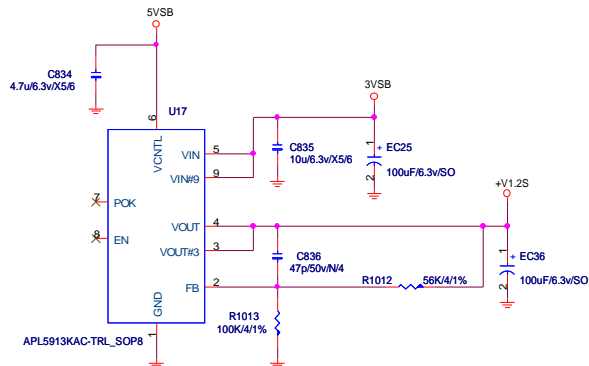
MICRO-STAR INT'L CO.,LTD			
MS-AC951			
Size Custom	Document Description	HDMI Out/ NFC /VGA PinHeader	
Date: Thursday, May 16, 2013	Sheet 29	of 49	

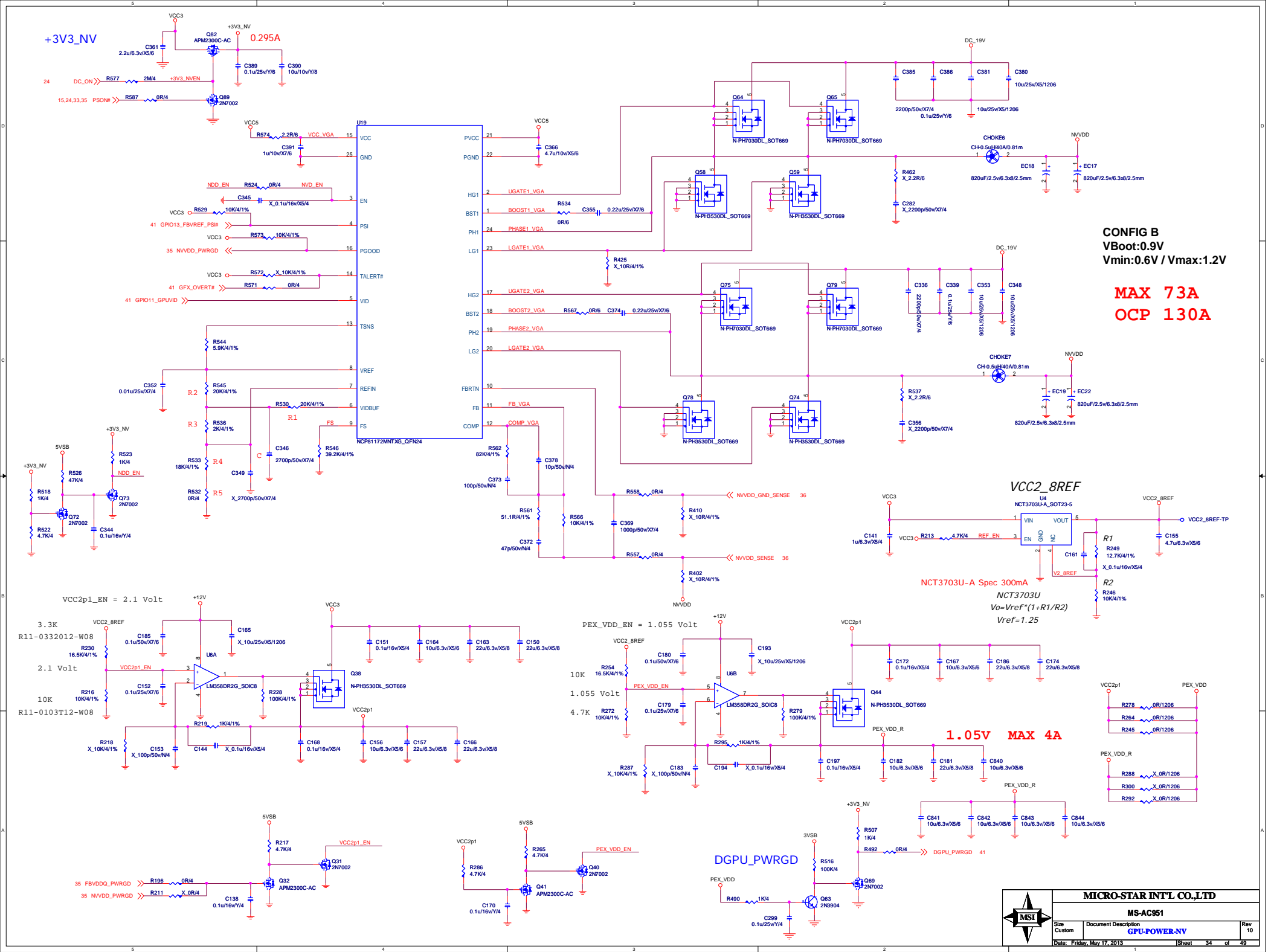
HDMI1 INPUT



COM PORT 1

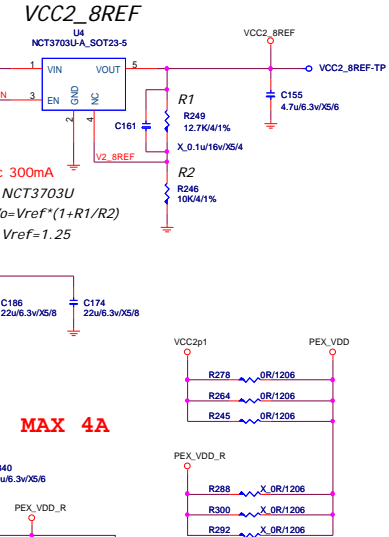


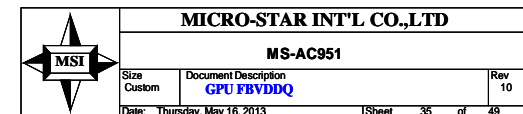
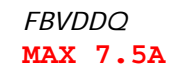




CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

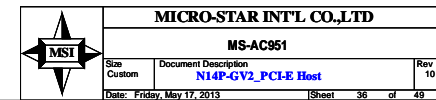
MAX 73A
OCP 130A



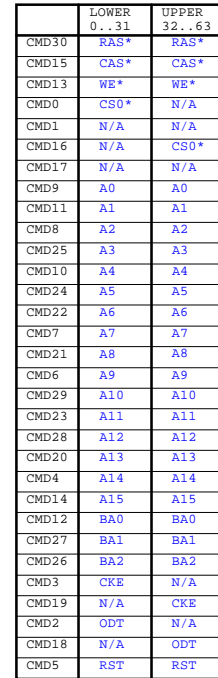


N14P-GV2 MSI PN:B03-0N14P65-N08
N14M-GE MSI PN:B03-0N14M15-N08

4x 10u, 4 x22u Place between GPU and Power Supply

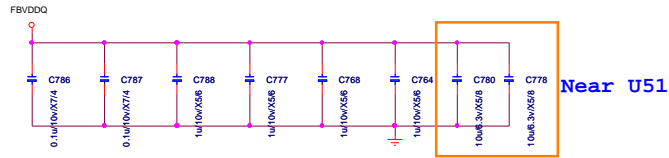


N14P-GV2 MSI PN:B03-0N14P65-N08
N14M-GE MSI PN:B03-0N14M15-N08

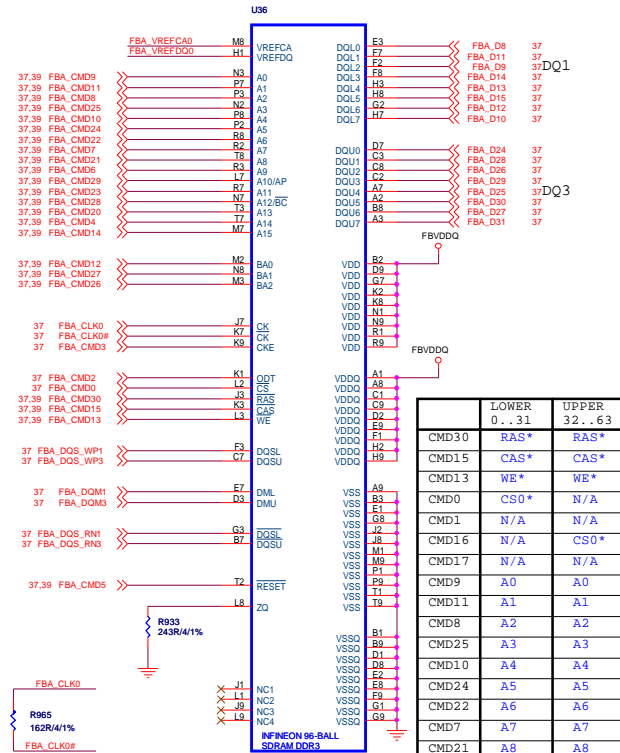


MEMORY DECOUPLING CAPS

DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



Near U51



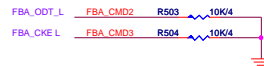
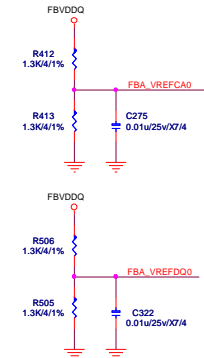
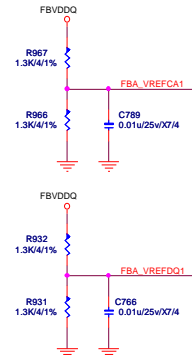
K4W4G1646B-HC11

M12-1646B15-S02

	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

* A15 is not required for any x16 device, even up to 4Gb density.

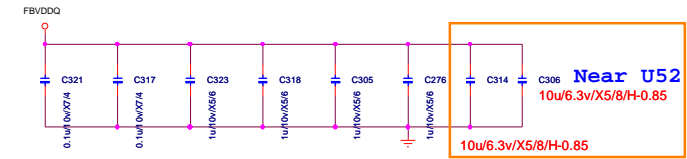
* A15 is only needed if we support x8 configurations, and only at 4Gb



GFX1X SDDR3 C4D MAPPING			
	D-31		32-43
	C30*		
CMD0			
CMD1			
CMD2	CDE		
CMD3	CKT		
CMD4	A14		A14
CMD5	B02		B02
CMD6	A8		A8
CMD7	A7		A7
CMD8	A2		A2
CMD9	A4		A4
CMD10	A1		A1
CMD11	A1		A1
CMD12	BA0		BA0
CMD13	WB*		WB*
CMD14	A15		A15
CMD15	CAS*		CAS*
CMD16			
CMD17	CSD		
CMD18			
CMD19	CME		
CMD20	A13		A13
CMD21	A8		A8
CMD22	A6		A6
CMD23	A11		A11
CMD24	A6		A6
CMD25	A3		
CMD26	BA2		BA2
CMD27	BA1		BA1
CMD28	A12		A12
CMD29	A10		A10
CMD30	BA0*		BA0*
CMD31			

MEMORY DECOUPLING CAPS

DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



C306 Near U52

10u/6.3v/X5/8/H-0.85

N14M-GS/LP AND N14P-GV2 DDR3 & DDR3L
MEMORY RVL

NVIDIA recommends the following DDR3 memories for use in conjunction with notebook designs using N14M-GS/LP and N14P-GV2.

Table 4. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories
128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
128M-16 D0R3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G-K	1000	1234	Production Candidate
				MT41J128M16JT-107G-K	900	1150	Production Candidate
	Hymix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate

Table 5. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories
256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
256Mx16 DOR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G-E	900	N/A	Production Candidate



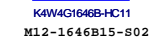
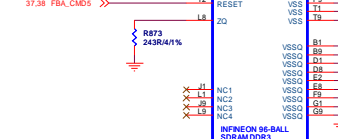
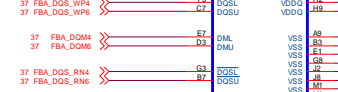
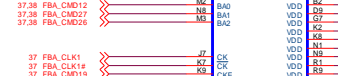
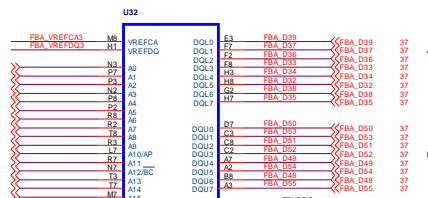
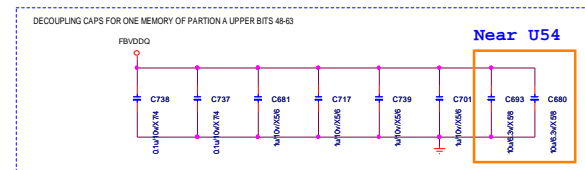
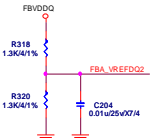
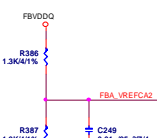
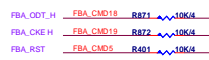
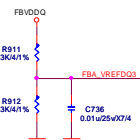
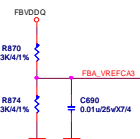
MICRO-STAR INT'L CO.,LTD

MS-AC951

Size Custom	Document Description FB Partition A bits 31..0
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Rev
10

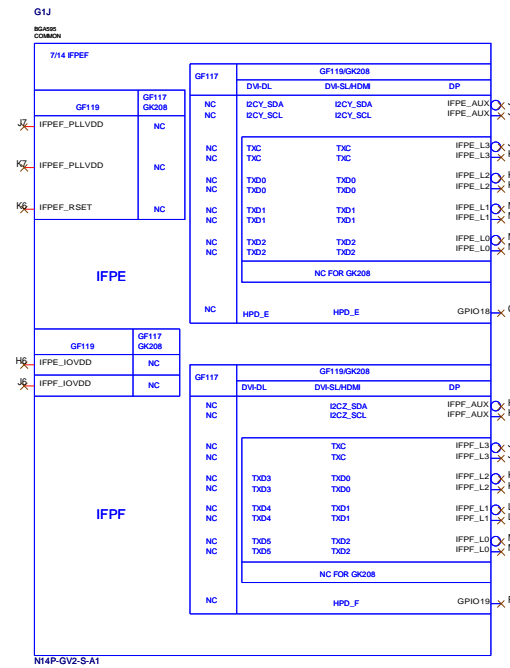
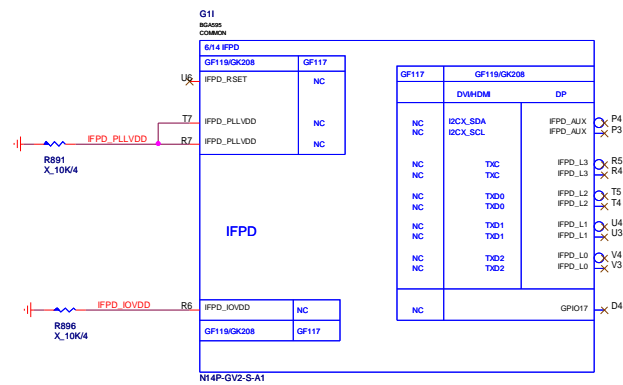
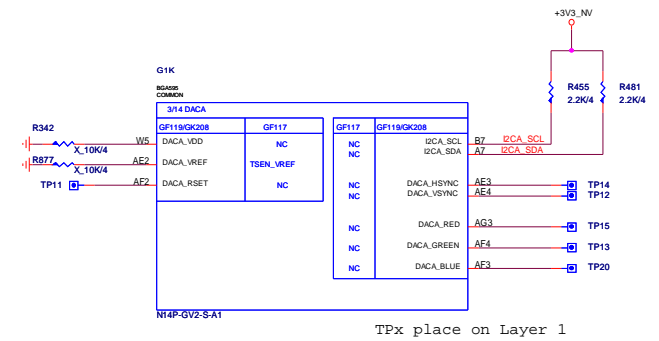
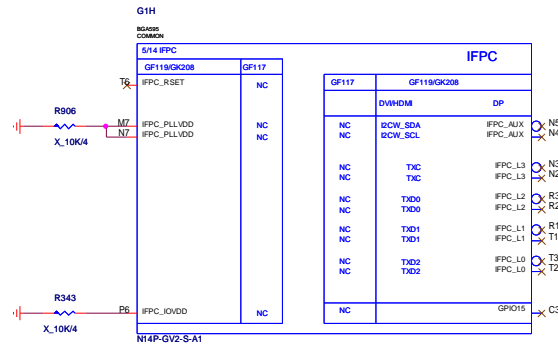
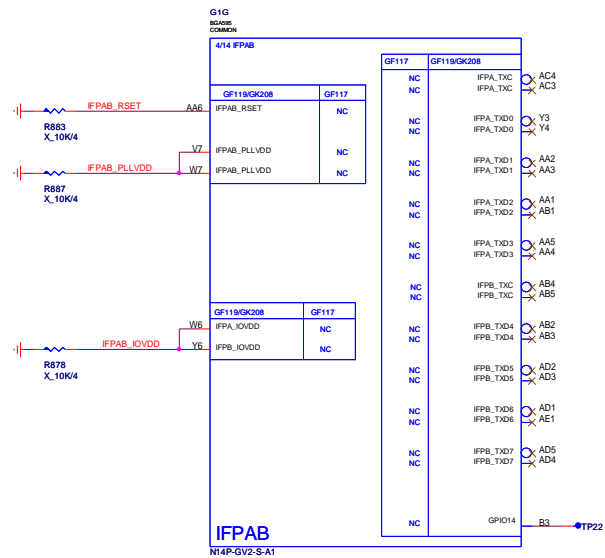
MEMORY DECOUPLING CAPS



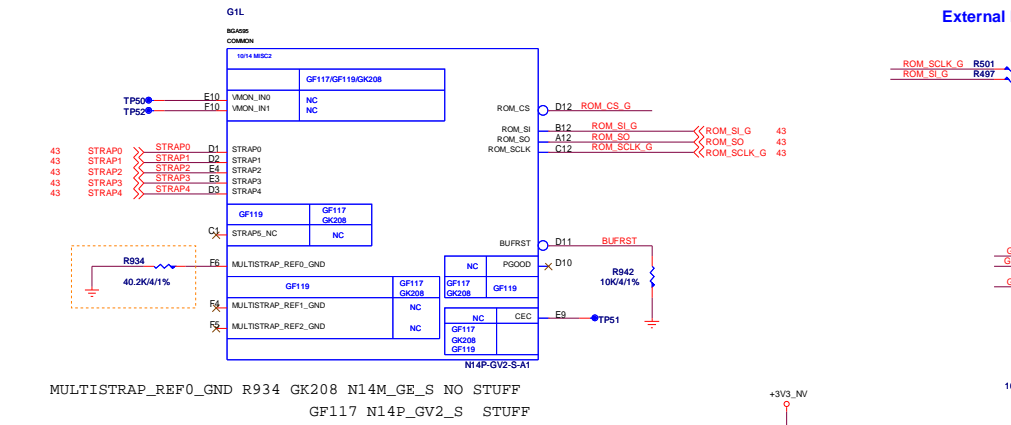
NVIDIA recommends the following DDR3 memories for use in conjunction with notebook designs using N14M-GS/LP and N14P-GV2.

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
128M-16 DGR3	Samsung	0x7	1.5 V	K4W20164E-BC1A	1000	1204	Production Candidate
			1.5 V	K4W20164E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V	MT4112M16J1T-093G-K	1000	1234	Production Candidate
			1.5 V	MT4112M16J1T-107G-K	1000	1150	Production Candidate
	Hynix	0x6	1.5V	H5TQ3G36FR-H0C	1000	N/A	Production Candidate
			1.5V	H5TQ3G36FR-11C	900	N/A	Production Candidate

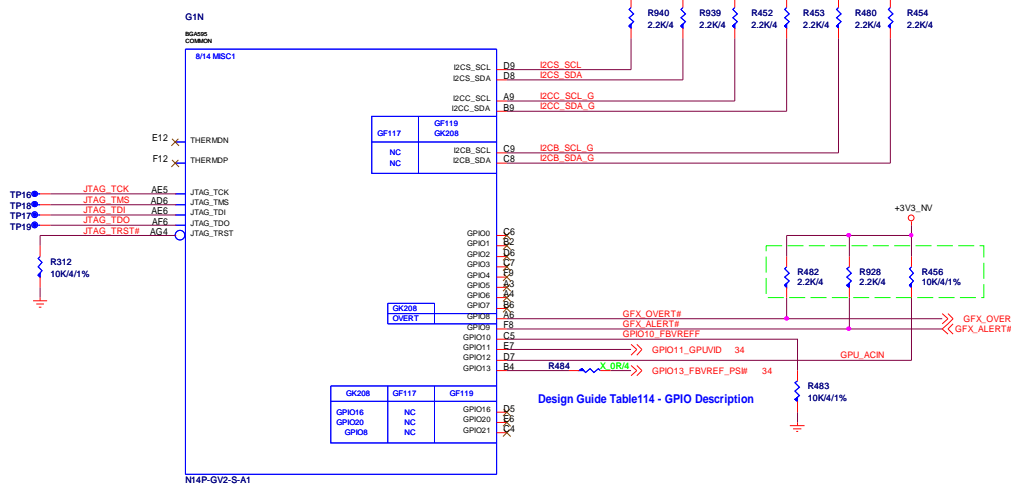
Configuration	Vendor	Strap	FBDVDD/ FBDVDDQ	Manufacturer Part Number	Max Speed Ck (MHz)	Memory Data Code Minimum	Status
256Mx16 DOR3	Samsung	Dx3	1.5 V/ 1.5 V	K4W4616-4GB-HC11	900	N/A	Production Candidate
	Micron	Dx1	1.5 V/ 1.5 V	MT41K256M16HA- 107G-E	900	N/A	Production Candidate



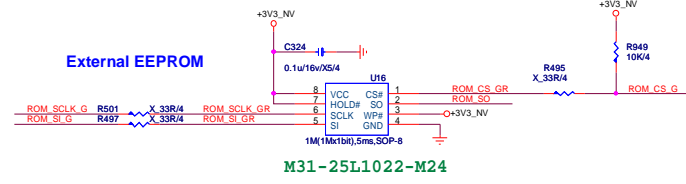
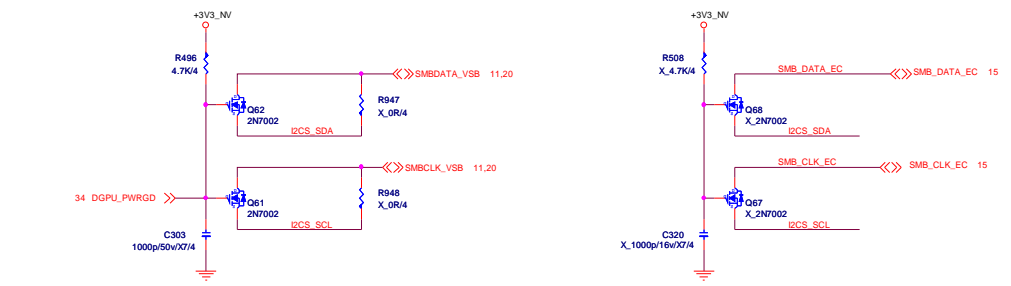
N14P-GV2 co-lay N14M-GE(Thermal & GPIO)



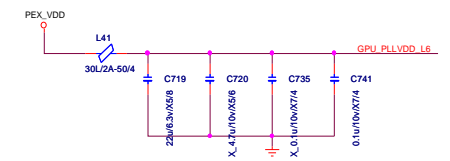
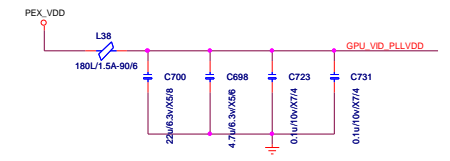
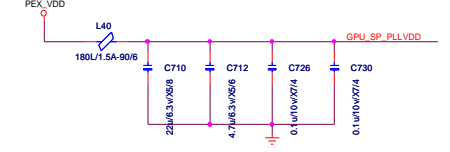
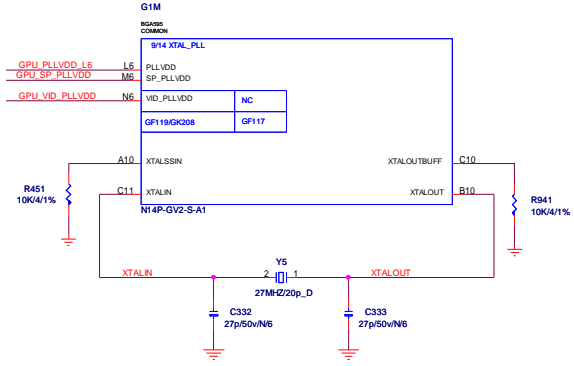
MULTISTRAP_REF0_GND R934 GK208 N14M_GE_S NO STUFF
GF117 N14P_GV2_S STUFF



Design Guide Table114 - GPIO Description

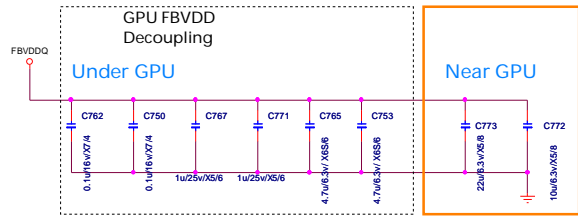


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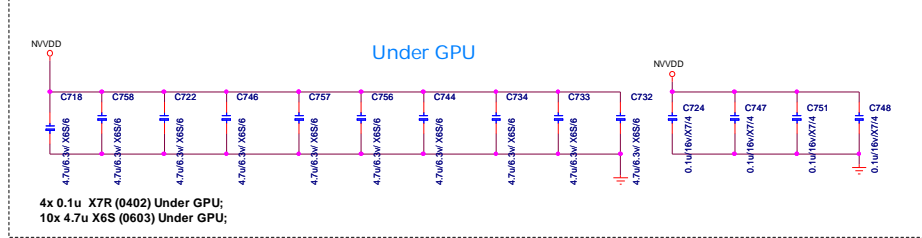


GPIO	GK208	GF117
GPIO 0	DEBUG Service	FAN_PWMFB_CLAMP/DEBUG Service
GPIO 1	MEM_VDD_CTL/FAN_PWM	NVVD_VID2
GPIO 2	LCD brightness control (LCD_BLPWM)	UNUSED
GPIO 3	LCD Power enable (LCD_PPEN)	UNUSED
GPIO 4	LCD Backlight enable (LCD_BLEN)	UNUSED
GPIO 5	NVVD PWM_VID_BOOT_EN	NVVD VID0
GPIO 6	Remote Sensor Error Correction	NVVD VID1
GPIO 7	LVDS_Switch3D VISION/STEREO	UNUSED
GPIO 8	GPU Overtemp	GPU Overtemp
GPIO 9	GPU thermal Alert	GPU Thermal Alert
GPIO 10	FB Vref Control	UNUSED
GPIO 11	NVVD PWM_VID	MEM_VDD_CTL
GPIO 12	PWR_Level AC Detect	PWR_Level AC Detect
GPIO 13	NVVD PSI	UNUSED(No Need to Set in VBIOS)
GPIO 14	HPD IFPAB (DPIM)	N/A on Package
GPIO 15	HPD IFPC (DP)	N/A on Package
GPIO 16	FAN_PWM	N/A on Package
GPIO 17	HPD IFPD (eDP)	N/A on Package
GPIO 18	UNUSED	N/A on Package
GPIO 19	HPD IFPF (DPIM)	N/A on Package
GPIO 20	UNUSED	N/A on Package
GPIO 21	UNUSED	N/A on Package

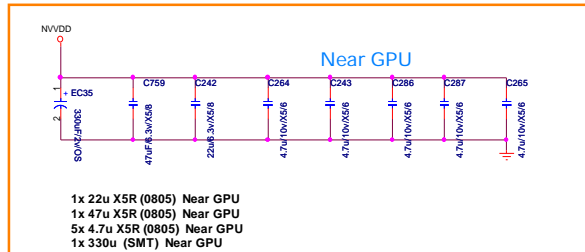
N14P-GV2 co-lay N14M-GE (Power & GND)



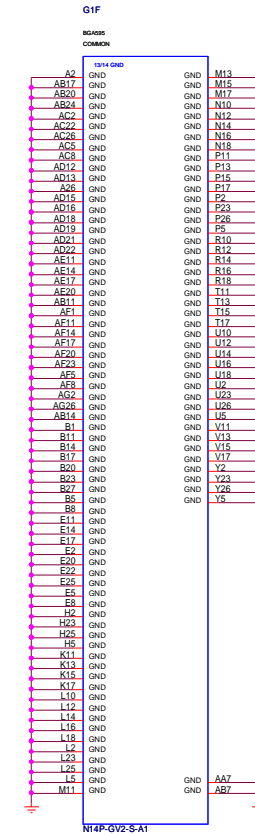
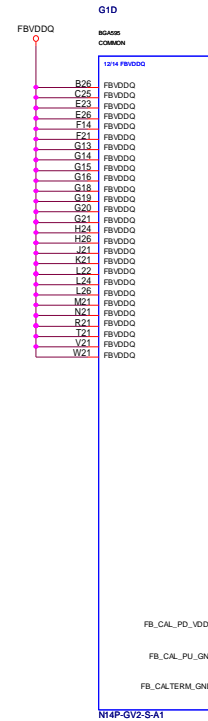
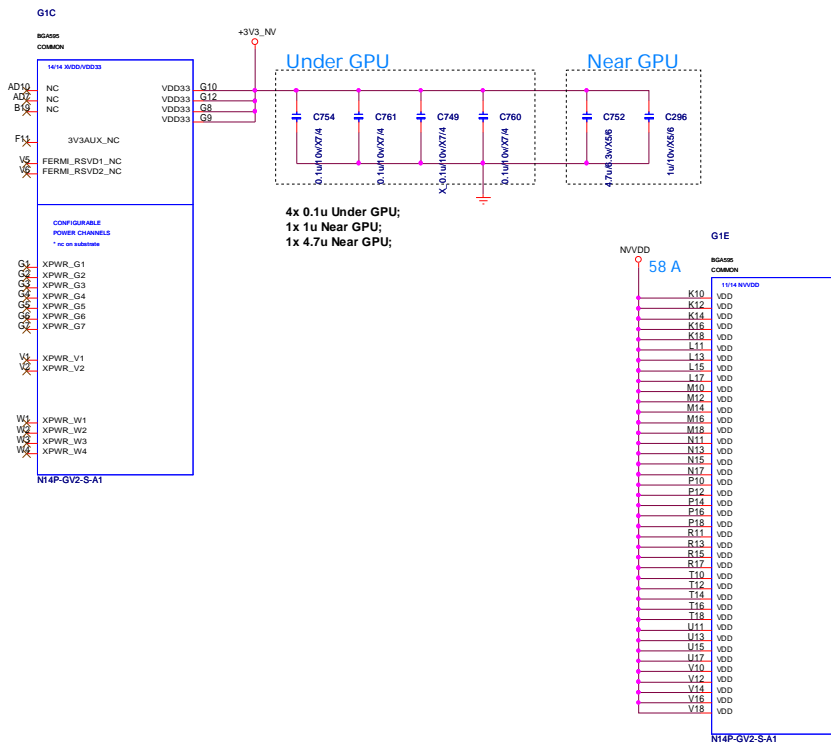
2x 0.1u X7R (0402) Under GPU;
2x 1u X7R (0603) Under GPU;
2x 4.7u X6S (0603) Under GPU;
1x 10u X5R (0805) Near GPU
1x 22u X5R (0805) Near GPU



4x 0.1u X7R (0402) Under GPU;
10x 4.7u X6S (0603) Under GPU;



1x 22u X5R (0805) Near GPU
1x 47u X5R (0805) Near GPU
5x 4.7u X5R (0805) Near GPU
1x 330u (SMT) Near GPU



Samsung 2G Die

N14M-GE/GL Strap0 10K PD

GMR1
X_10K/4/1%

N14M-GE/GL Strap1 10K PD

GMR4
X_10K/4/1%

N14M-GE/GL Strap2 10K PU

GMR2
X_10K/4/1%

N14M-GE/GL Strap3 10K PD

GMR5
X_10K/4/1%

N14M-GE/GL Strap4 10K PD

GMR3
X_10K/4/1%N14M-GS/LP AND N14P-GV2 DDR3 & DDR3L
MEMORY RVL

NVIDIA recommends the following DDR3 memories for use in conjunction with notebook designs using N14M-GS/LP and N14P-GV2.

Table 4. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories
128Mx16 Configuration

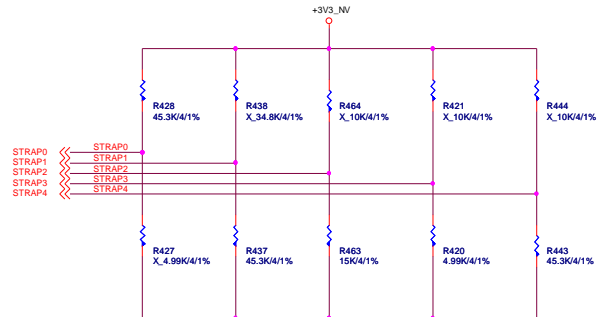
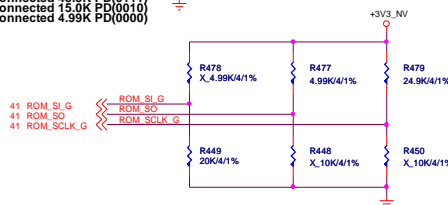
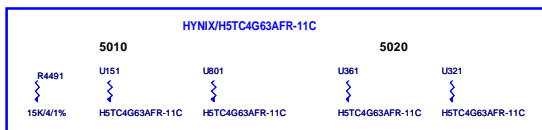
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT- 093G-K	1000	1234	Production Candidate
				MT41J128M16JT- 107G-K	900	1150	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate

Table 5. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories
256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
				MT41K256M16HA- 107G-E	900	N/A	Production Candidate

Table 6. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories
256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
				MT41K256M16HA- 107G-E	900	N/A	Production ready
	Hynix	0x2	1.5V/ 1.5V	H5TC4G63AFR-11C	900	N/A	Production- ready

STRAP1 should be connected 45.3K PD(0111)
STRAP2 should be connected 15.3K PD(0010)
STRAP3 should be connected 4.99K PD(0000)ROM_SCLK should be connected 24.9K PU (1100) for N14P-GV2
10K PD for N14M-GE/GLROM_SO should be connected 4.99K PU(1000) for N14P-GV2
10K PD for N14M-GE/GLROM_SI should be connected 20K PD(0011) Samsung K4W4G1646B-HC11 for N14P-GV2 256Mx16
20K PD(0011) Samsung K4W4G1646B-HC11 for N14M-GE/GL 256Mx16

GF11X/GK208 STRAP PIN MODE TABLE				
PIN NAME	MULTI-LEVEL bit [3:0] Bit 3	Bit 2	Bit 1	Bit 0
STRAP0	USER [3]	USER [2]	USER [1]	USER [0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP2	PCI_DEVID [3]	PCI_DEVID [2]	PCI_DEVID [1]	PCI_DEVID [0]
STRAP3	SOR[3]_EXPOSED	SOR[2]_EXPOSED	SOR[1]_EXPOSED	SOR[0]_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
ROM_SCLK	PCI_DEVID [4]	SUB_VENDOR	PCI_DEVID [5]	PEX_PLL_EN_TERM
ROM_SI	RAMCFG [3]	RAMCFG [2]	RAMCFG [1]	RAMCFG [0]
ROM_SO	FB [1]	FB [0]	SMB_ALT_ADDR	VGA_DEVICE

GND			3V3
4.99K	0000	1000	
10K	0001	1001	
15K	0010	1010	
20K	0011	1011	
24.9K	0100	1100	
30.1K	0101	1101	
34.8K	0110	1110	
45.3K	0111	1111	

RAM_CFG[3:0] Definitions

GK208/GK107: MEMORY STRAP TABLE

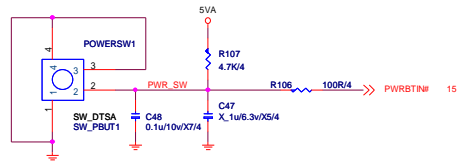
0001 256Mx16 SDDR3 Micron
0010 256Mx16 SDDR3 Samsung
0011 256Mx16 SDDR3 Samsung
0100 128Mx16 SDDR3 Micron
0101 128Mx16 SDDR3 Micron
0110 128Mx16 SDDR3 Hynix
0111 128Mx16 SDDR3 Samsung

USER_BIT0	Default All SKU(s):	
USER_BIT1	0xF = 45K PU	
USER_BIT2	LVDS Panel EDID Mode	
USER_BIT3		
3GIO_PADCFG 0	Table 131 3GIO_PADCFG Strap Settings	
3GIO_PADCFG 1	0110 Gen 1 / Gen 2 support only	
3GIO_PADCFG 2	0000 Gen 3 support	
3GIO_PADCFG 3		
PCI_DEVID_0	PCDEVID_3[0] Definitions (Note Actual DEVID set also depends on PCI_DEVID_4)	
PCI_DEVID_1		
PCI_DEVID_2		
PCI_DEVID_3		
VGA_DEVICE	0: 3D DEVICE 1: VGA DEVICE	
SMB_ALT_ADDR	0: Thermal Sensor ADR = 0x9E (Default) 1: Thermal Sensor ADR = 0x9C (Multi-GPU usage)	
FB [1:0]	10 : 256 MB (Default) Table 125 N14X FB Aperture Size	
RAM_CFG_0		
RAM_CFG_1		
RAM_CFG_2		
RAM_CFG_3		
PEX_PLL_EN_TERM	0: DISABLED (Default) 1: Enable	
SUB_VENDOR	0: No Video BIOS ROM 1: BIOS ROM IS PRESENT (Default)	
DP_PLL_VDD33V	0: Reserved 1: Default	
PCIE_MAX_SPEED	0: Limit booting to PCIE Gen 1 1: Allow booting to PCIE Gen 2 / 3	
PCIE_SPEED_CHANGE_GEN3	0: Disable PCIE Gen 3 operation 1: Enable PCIE Gen 3 operation	
SOR[X]_EXPOSED	0000 : Not in use	

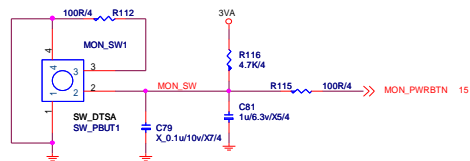


MICRO-STAR INT'L CO.,LTD			
MS-AC951			
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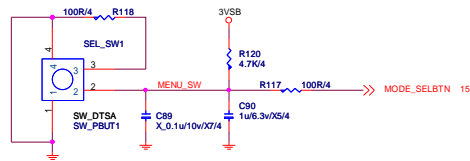
POWER ON/OFF BUTTON



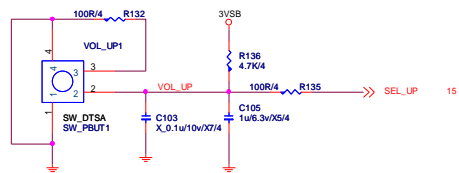
HDMI IN / PC / Monitor OFF BUTTON



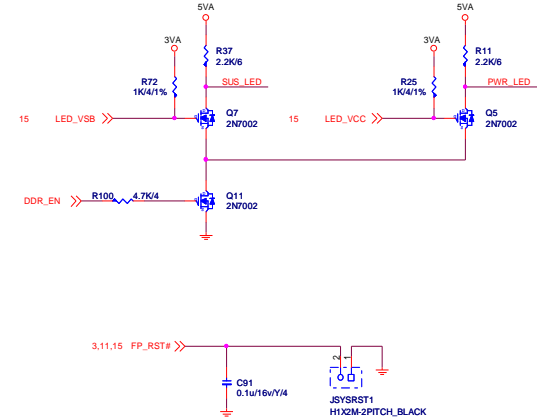
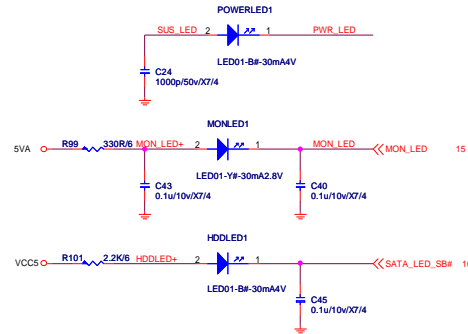
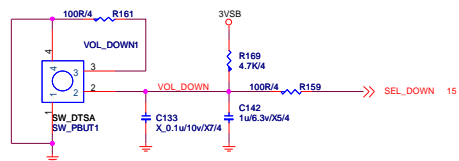
OSD MODE SELECT BUTTON



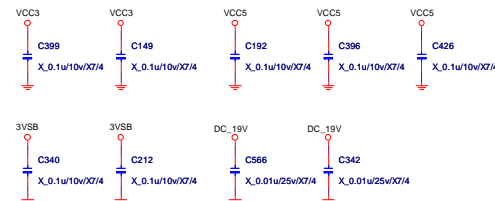
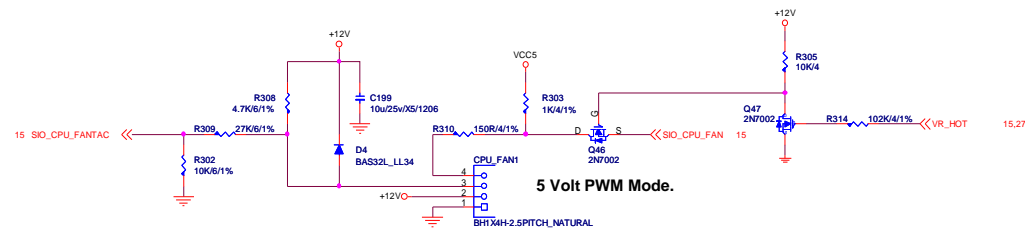
ITEM UP CONTROL

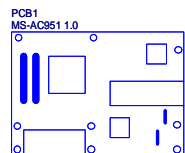


ITEM DOWN CONTROL



SYSTEM FAN

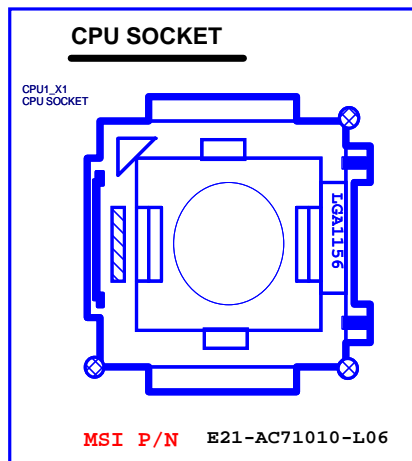




P80-AC95110-E48
P80-AC95110-G37

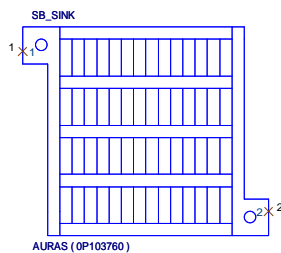


LABEL1
BIOS
Label
BIOS LABEL

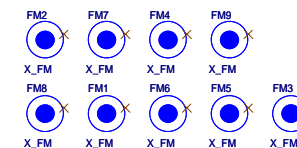


LABEL2
HDMI ROYALTY
HDMI_ROYALTY_0.15

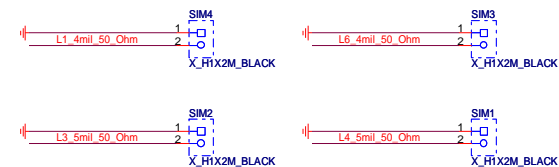
CPU_BK1
CPU_backplate



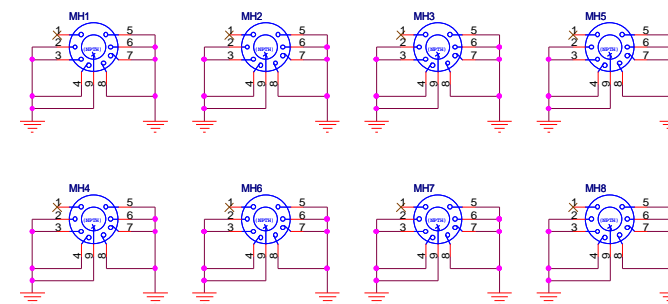
Optical Fiducial Marks-120



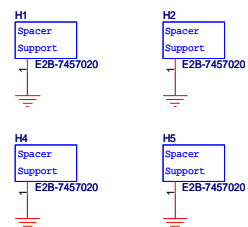
Simulation Single End 50ohm



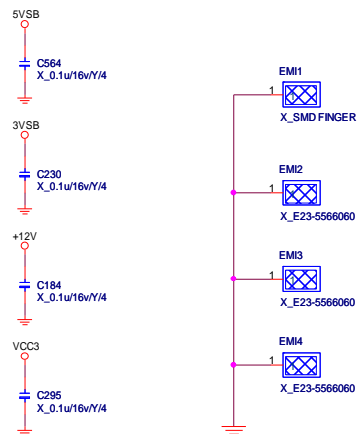
Mounting Holes



GPU Stand off



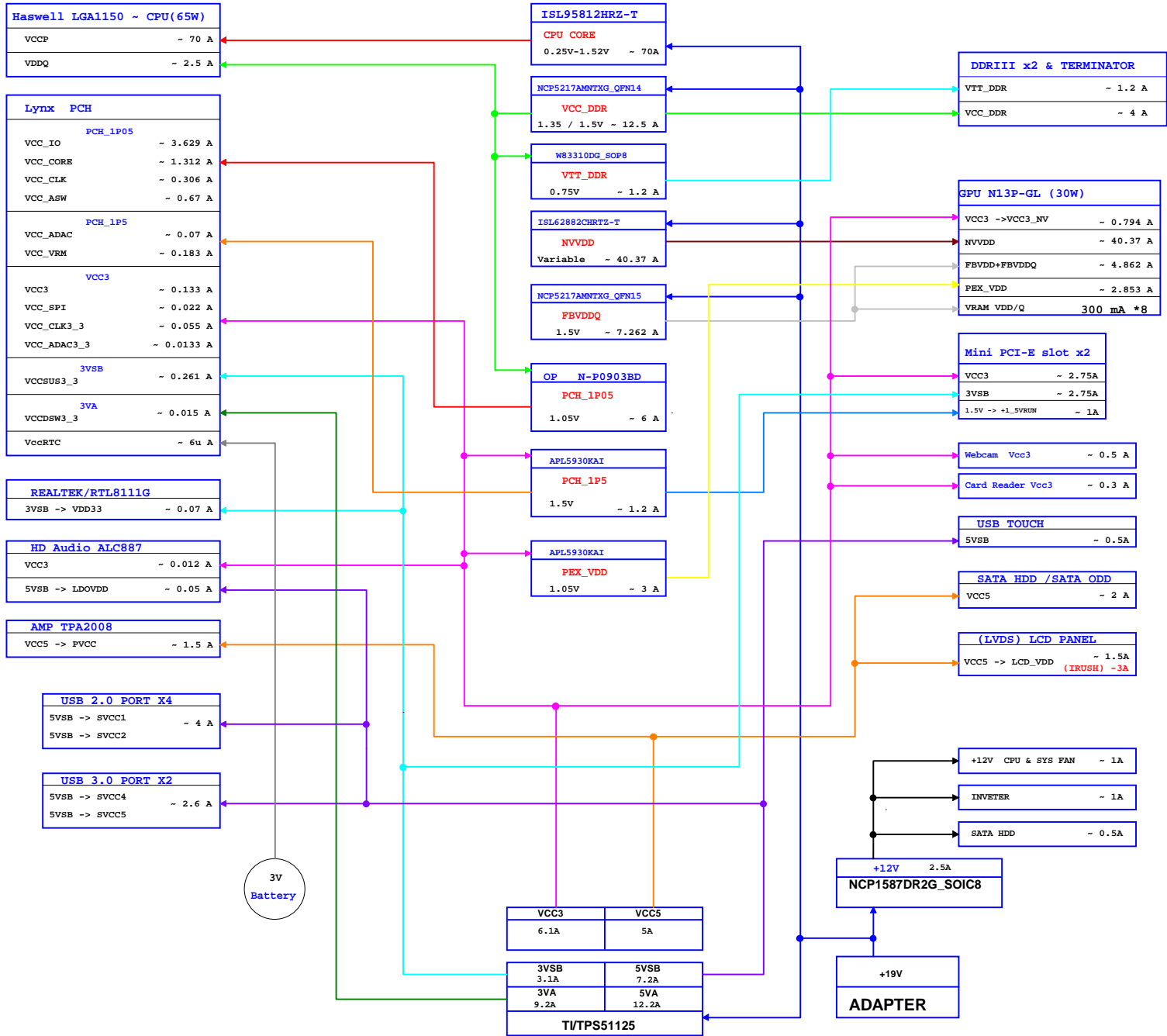
EMI



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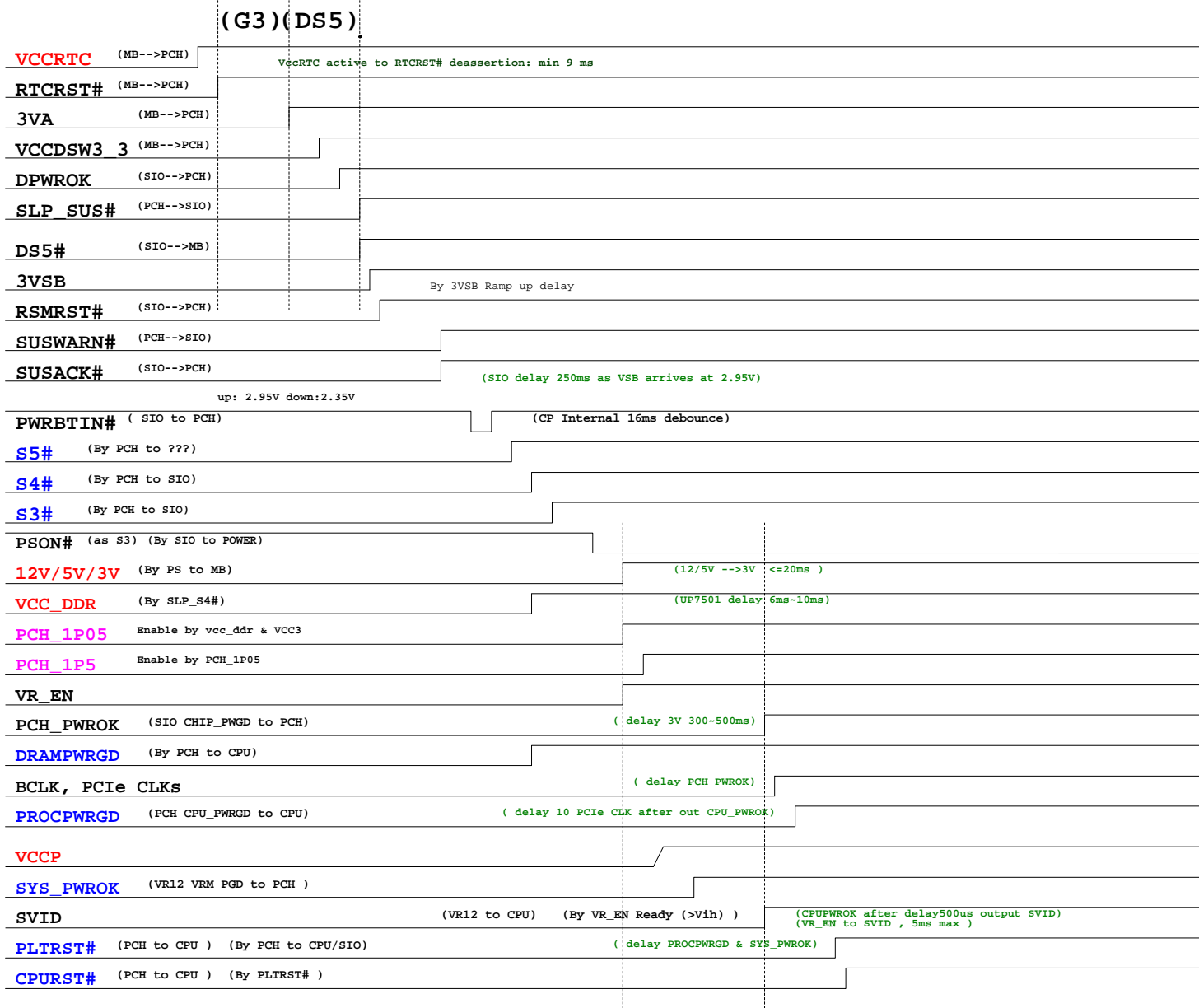
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Lynx Point Platform

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO0	BMBUSY#	I/O	CORE	Y	3.3V	GPI	BM_BUSY#	Pull-up 10K to VCC3	No USE
GPIO1	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	WLAN2_PWRON	Pull-up 10K to VCC3	WLAN2_PWRON
GPIO2	PIRQE#	I/OD	CORE	Y	5V	GPI	PCH_GPIO2	Pull-up 4.7K to VCC3	MON_PWRBTN
GPIO3	PIRQF#	I/OD	CORE	Y	5V	GPI	PCH_GPIO3	Pull-up 10K to VCC3	D-MC
GPIO4	PIRQG#	I/OD	CORE	Y	5V	GPI	PCH_GPIO4	Pull-up 4.7K to VCC3	MODE_SELBTN
GPIO5	PIRQH#	I/OD	CORE	Y	5V	GPI	PCH_GPIO5	Pull-up 4.7K to VCC3	SEL_UP
GPIO6	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	PCH_GPIO6	Pull-up 4.7K to VCC3	SEL_DOWN
GPIO7	Unmultiplexed	I/O	CORE	Y	3.3V	GPI	PCH_GPIO7	Pull-up 10K to VCC3	No USE
GPIO8	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	ICC_EN	Pull-down	STRAP
GPIO9	OC3#	I/O	Suspend	Y	3.3V	Native	OC#5	Pull-up 10K to 3VSB	OC3#
GPIO10	OC6#	I/O	Suspend	Y	3.3V	Native	OC#6	Pull-up 10K to 3VSB	OC6#
GPIO11	SMBALERT#	I/O	Suspend	Y	3.3V	Native	PCH_SMBALERT#	Pull-up 10K to 3VSB	No USE
GPIO12	LAN_PHY_PWR_CTRL	I/O	DSW	Y	3.3V	Native	PCH_GPIO12	N/A	No USE
GPIO13	HDA_DOCK_RST#	I/O	Suspend	Y	3.3V	GPI	PCH_GPIO13	Pull-up 10K to 3VSB	No USE
GPIO14	OC7#	I/O	Suspend	Y	3.3V	Native	PCH_GPIO14	Pull-up 10K to 3VSB	MON_LED
GPIO15	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	PCH_GPIO15	N/A	CHARGER_EN
GPIO16	SATA4GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO16	Pull-up 10K to VCC3	No USE
GPIO17	Unmultiplexed	I/O	CORE	N	3.3V	GPI	WLAN1_PWRON	Pull-up 10K to VCC3	WLAN1_PWRON
GPIO18	PCIECLKRQ1#	I/O	CORE	N	3.3V	Native	PCIECLKRQ1#	Pull-up 10K to VCC3	PCIECLKRQ1#
GPIO19	SATA1GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO19	Pull-up 10K to VCC3	STRAP
GPIO20	PCIECLKRQ2#	I/O	CORE	N	3.3V	Native	PCIECLKRQ2#	Pull-up 10K to VCC3	PCIECLKRQ2#
GPIO21	SATA0GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO21	Pull-up 10K to VCC3	No USE
GPIO22	SCLCK	I/O	CORE	N	3.3V	GPI	PCH_GPIO22	Pull-up 10K to VCC3	No USE
GPIO23	LDRQ1#	I/O	CORE	N	3.3V	Native	NC	N/A	No USE
GPIO24	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO24	N/A	CHARGER_S0
GPIO25	PCIECLKRQ3#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ3#	Pull-up 10K to 3VSB	PCIECLKRQ3#
GPIO26	PCIECLKRQ4#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ4#	Pull-up 10K to 3VSB	PCIECLKRQ4#
GPIO27	Unmultiplexed	I/O	DSW	N	3.3V	GPI	PCH_GPIO27	Pull-up 10K to 3VA	No USE
GPIO28	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO28	N/A	CHARGER_S1
GPIO29	SLP_LAN#	I/O	DSW	N	3.3V	Native	PCH_GPIO29	N/A	No USE
GPIO30	SUSWARN# SUSWRNACK	I/O	Suspend	N	3.3V	Native	SUSWARN#	N/A	SUSWARN#
GPIO31	Unmultiplexed	I/O	DSW	N	3.3V	GPI	PCH_GPIO31	Pull-up 10K to 3VA	No USE
GPIO32	only CLKRUN#	I/O	CORE	N	3.3V	GPO	PCH_GPIO32	N/A	No USE
GPIO33	HDA_DOCK_EN#	I/O	CORE	N	3.3V	GPO	PCH_GPIO33	N/A	No USE
GPIO34	Unmultiplexed	I/O	CORE	N	3.3V	GPI	STP_PC#	Pull-up 10K to VCC3	STP_PC#
GPIO35	NM#	I/O	CORE	N	3.3V	GPO	PCH_GPIO35	N/A	DDR_VCTL
GPIO36	SATA2GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO36	N/A	STRAP
GPIO37	SATA3GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO37	Pull-up 10K to VCC3	STRAP
GPIO38	SLOAD	I/O	CORE	N	3.3V	GPI	PCH_GPIO38	Pull-up 10K to VCC3	No USE
GPIO39	SDATAOUT0	I/O	CORE	N	3.3V	GPI	PCH_GPIO39	Pull-up 10K to VCC3	No USE
GPIO40	OC1#	I/O	Suspend	N	3.3V	Native	OC#1	Pull-up 10K to 3VSB	OC1#
GPIO41	OC2#	I/O	Suspend	N	3.3V	Native	OC#2	Pull-up 10K to 3VSB	OC2#
GPIO42	OC3#	I/O	Suspend	N	3.3V	Native	OC#3	Pull-up 10K to 3VSB	OC3#
GPIO43	OC4#	I/O	Suspend	N	3.3V	Native	OC#4	Pull-up about 3VSB	OC4#
GPIO44	PCIECLKRQ5#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ5#	Pull-up 10K to 3VSB	PCIECLKRQ5#
GPIO45	PCIECLKRQ6#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ6#	Pull-up 10K to 3VSB	PCIECLKRQ6#

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO46	PCIECLKRQ7#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ7#	Pull-up 10K to 3VSB	PCIECLKRQ7#
GPIO47	is not available	I/O	Suspend	N	3.3V	Native			
GPIO48	SDATAOUT1	I/O	CORE	N	3.3V	GPI	PCH_GPIO48	Pull-up 10K to VCC3	No USE
GPIO49	SATA5GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO49	Pull-up 10K to VCC3	No USE
GPIO50	Unmultiplexed	I/O	CORE	N	5V	GPI	PCH_GPIO50	Pull-up 10K to VCC3	No USE
GPIO51	Unmultiplexed	I/O	CORE	N	3.3V	GPO	PCH_GPIO51	N/A	STRAP
GPIO52	Unmultiplexed	I/O	CORE	N	5V	GPI	PCH_GPIO52	Pull-up 10K to VCC3	No USE
GPIO53	Unmultiplexed	I/O	CORE	N	3.3V	GPO	PCH_GPIO53	N/A	STRAP
GPIO54	Unmultiplexed	I/O	CORE	N	5V	GPI	PCH_GPIO54	Pull-up 10K to VCC3	No USE
GPIO55	Unmultiplexed	I/O	CORE	N	3.3V	GPO	PCH_GPIO55	N/A	STRAP
GPIO56	is not available	I/O	Suspend	N	3.3V	Native			
GPIO57	Unmultiplexed	I/O	Suspend	N	3.3V	GPI	PCH_GPIO57	Pull-up 10K to 3VSB	NFC
GPIO58	SML1CLK	I/O	Suspend	N	3.3V	Native	PCH_SML1CLK	Pull-up 2.2K to 3VSB	PCH_SML1CLK
GPIO59	OC0#	I/O	Suspend	N	3.3V	Native	OC#0	Pull-up 10K to 3VSB	OC0#
GPIO60	SML0ALERT#	I/O	Suspend	N	3.3V	Native	PCH_SML0ALERT#	Pull-up 10K to 3VSB	No USE
GPIO61	SUS_SATA#	I/O	Suspend	N	3.3V	Native	SUS_STAT#	N/A	No USE
GPIO62	SUSCLK	I/O	Suspend	N	3.3V	Native	SUS_CLK	N/A	No USE
GPIO63	SLP_S5#	I/O	Suspend	N	3.3V	Native	SLP_S5#	N/A	No USE
GPIO64	CLKOUTFLEX0	I/O	CORE	N	3.3V	Native	NC	N/A	No USE
GPIO65	CLKOUTFLEX1	I/O	CORE	N	3.3V	Native	CK_48M_FLEX1	N/A	CK_48M_SIO
GPIO66	CLKOUTFLEX2	I/O	CORE	N	3.3V	Native	NC	N/A	No USE
GPIO67	CLKOUTFLEX3	I/O	CORE	N	3.3V	Native	CK_48M_FLEX3	N/A	CK_48M_CARD
GPIO68	Unmultiplexed	I/O	CORE	N	3.3V	GPI	PCH_GPIO68	Pull-up 10K to VCC3	No USE
GPIO69	Unmultiplexed	I/O	CORE	N	3.3V	GPI	PCH_GPIO69	Pull-up 10K to VCC3	No USE
GPIO70	Unmultiplexed	I/O	CORE	N	3.3V	Native	PCH_GPIO70	Pull-up 10K to VCC3	No USE
GPIO71	Unmultiplexed	I/O	CORE	N	3.3V	Native	PCH_GPIO71	Pull-up 10K to VCC3	No USE
GPIO72	BATLOW#	I/O	DSW	N	3.3V	Native	PCH_GPIO72	Pull-up 1K to 3VA	No USE
GPIO73	PCIECLKRQ0#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ0#	Pull-up 10K to 3VSB	PCIECLKRQ0#
GPIO74	SMBALERT# PCHHOT#	I/O	Suspend	N	3.3V	Native	PCH_SML1ALERT#	Pull-up 10K to 3VSB	NFC
GPIO75	SML1DATA	I/O	Suspend	N	3.3V	Native	PCH_SML1DATA	Pull-up 2.2K to 3VSB	PCH_SML1DATA



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AIO MS-AC951 Version 1.0 SCHEMATIC HISTORY

Rev	Date	Page	Description
1.0	20130422	19	JHDDPWR1 change footprint and P/N : N32-1040D31-H06.
1.0	20130422	23	R707 from 1206 change to 0603.
1.0	20130422	27	Modify Gate and Phase circuit error.
1.0	20130422	45	Add HDMI In / Out Label.
1.0	20130422	9	C236 and C237 footprint from 0402 change to 0603.
1.0	20130422	16	C462 and C832 footprint from 0402 change to 0603.
1.0	20130422	17	C549 and C551 footprint from 0402 change to 0603.
1.0	20130422	18	C293 and C294 footprint from 0402 change to 0603.
1.0	20130422	41	C332 and C333 footprint from 0402 change to 0603.
1.0	20130422	21	Q90 from 2N3904 change to 2N7002.
1.0	20130422	19	R442 change to NC.
1.0	20130422	27	Q10 from 2N3904 change to APM2300C.
1.0	20130424	16	R999 , R1000 , C494 NC , Add R1011 1K Ohm for S5 VCC5 leakage.
1.0	20130424	32	U17 change to APL5913 SOP8 for thermal issue.
1.0	20130424	26	R301 from 10.7K change to 11K.
1.0	20130425	25	EC1 , Q124 change to NC for Power team suggest.
1.0	20130425	27	C37 from 33pf change to 100pf for power team suggest.
1.0	20130425	28	EC6 , EC7, EC11 change to NC for Power team suggest.
1.0	20130425	3	R52 from 0402 change to 0603, remove R39.
1.0	20130425	7	Add R1014 , C837, R1015 , R1016 , C838 , R1017 for DDR VREF.
1.0	20130425	8	Delete M_VREF_DQ_DIMM1 ; Add R1018 , C839 , R1019 for DDR VREF..
1.0	20130430	19	R423 NC ; R417 net from CHARGER_EN change to PPON2_EN , Avoid 5VSB leakage 0.3 volt.
1.0	20130506	29	Remove Q100 , R1004 , R614 , R625 , R626 , Q103 , C450 , R633 , R630 , R654 , R648. Add Q136 , Q137 , R1020 , R1021 , R1022 for HDMI OUT HPD.
1.0	20130508	16	PVCC change to 5VSB for HDMI in put audio, L56 change to NC.
1.0	20130510	11	Add R1023 for Quicksetting.
1.0	20130510	31	Y4 From DIP change to SMD for reduese ESR from 50 Ohm to 30 Ohm. C300 , C319 from 22pF change to 30pF.
1.0	20130510	35	Remove U21 circuit , because U21 over spec.
1.0	20130513	34	Delete C198 卡Thermal module, add C840 ~ C844.
1.0	20130513	11	C131 , C136 from 15pF change to 12pF.
1.0	20130513	41	C332 , C333 from 22pF change to 27pF.
1.0	20130513	21	Y6 from DIP change to SMD, C392, C393 from 16pF change to 27pF.
1.0	20130514	15	C638 from 15pF change to 12pF.



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